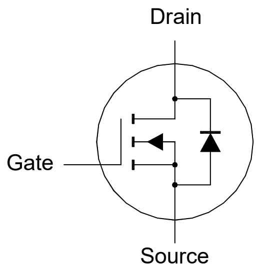
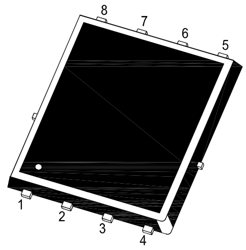
WTM506N750LS-HAF

N-Channel Enhancement Mode MOSFET

Features
- Low threshold drive
- Halogen and Antimony Free(HAF), RoHS compliant





1.Source 2.Source 3.Source 4.Gate
5.Drain 6.Drain 7.Drain 8.Drain
DFN5060 Plastic Package

Applications
- Switching applications
- DC-DC converters for Telecom and Computer

Key Parameters

Parameter	Value	Unit
BV_{DSS}	60	V
$R_{DS(ON)}$ Max	75 @ V_{GS} = 10 V	mΩ
	90 @ V_{GS} = 4.5 V	
$V_{GS(th)}$ typ	1.7	V
Q_g typ	8 @ V_{GS} = 10 V	nC

Absolute Maximum Ratings (at T_a = 25℃ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current T_c = 25℃	I_D	9.3	A
Drain Current T_c = 100℃		5.8	
Peak Drain Current, Pulsed [1)]	I_{DM}	20	A
Single-Pulse Avalanche Current	I_{AS}	5.6	A
Single-Pulse Avalanche Energy [2)]	E_{AS}	1.5	mJ
Power Dissipation T_c = 25℃	P_D	13.4	W
Operating Junction and Storage Temperature Range	T_j, T_{stg}	- 55 to + 150	℃

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance - Junction to Case	$R_{\theta JC}$	9.3	℃/W
Thermal Resistance - Junction to Ambient [3)] Steady State	$R_{\theta JA}$	48	℃/W

[1)] Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 2%, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C.

[2)] Limited by $T_{J(MAX)}$, starting T_J = 25 °C, L = 0.1 mH, R_g = 25 Ω, I_{AS} = 5.6 A, V_{GS} = 10 V.

[3)] Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

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Characteristics at T_a = 25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I_D = 250 µA	BV_{DSS}	60	-	-	V
Drain-Source Leakage Current at V_{DS} = 48 V	I_{DSS}	-	-	1	µA
Gate Leakage Current at V_{GS} = ± 20 V	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at V_{DS} = V_{GS}, I_D = 250 µA	$V_{GS(th)}$	1.2	-	2.5	V
Drain-Source On-State Resistance at V_{GS} = 10 V, I_D = 2 A at V_{GS} = 4.5 V, I_D = 1.5 A	$R_{DS(on)}$	- -	60 -	75 90	mΩ
DYNAMIC PARAMETERS					
Forward Transconductance at V_{DS} = 5 V, I_D = 2 A	g_{FS}	-	4.2	-	S
Gate Resistance at V_{DS} = 0 V, V_{GS} = 0 V, f = 1 MHz	R_g	-	1.3	-	Ω
Input Capacitance at V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz	C_{iss}	-	445	-	pF
Output Capacitance at V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz	C_{oss}	-	22	-	pF
Reverse Transfer Capacitance at V_{DS} = 30 V, V_{GS} = 0 V, f = 1 MHz	C_{rss}	-	18	-	pF
Gate Charge Total at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 2 A at V_{DS} = 30 V, V_{GS} = 4.5 V, I_D = 2 A	Q_g	- -	8 4	- -	nC
Gate to Source Charge at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 2 A	Q_{gs}	-	1.8	-	nC
Gate to Drain Charge at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 2 A	Q_{gd}	-	1.2	-	nC
Turn-On Delay Time at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 2 A, R_g = 4.7 Ω	$t_{d(on)}$	-	7	-	ns
Turn-On Rise Time at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 2 A, R_g = 4.7 Ω	t_r	-	2	-	ns
Turn-Off Delay Time at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 2 A, R_g = 4.7 Ω	$t_{d(off)}$	-	6	-	ns
Turn-Off Fall Time at V_{DS} = 30 V, V_{GS} = 10 V, I_D = 2 A, R_g = 4.7 Ω	t_f	-	5	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I_S = 1 A, V_{GS} = 0 V	V_{SD}	-	-	1.2	V
Body-Diode Continuous Current	I_S	-	-	9.3	A
Body-Diode Continuous Current, Pulsed	I_{SM}	-	-	20	A
Body Diode Reverse Recovery Time at I_S = 2 A, di/dt = 100 A / µs	t_{rr}	-	8.3	-	ns
Body Diode Reverse Recovery Charge at I_S = 2 A, di/dt = 100 A / µs	Q_{rr}	-	4.3	-	nC

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

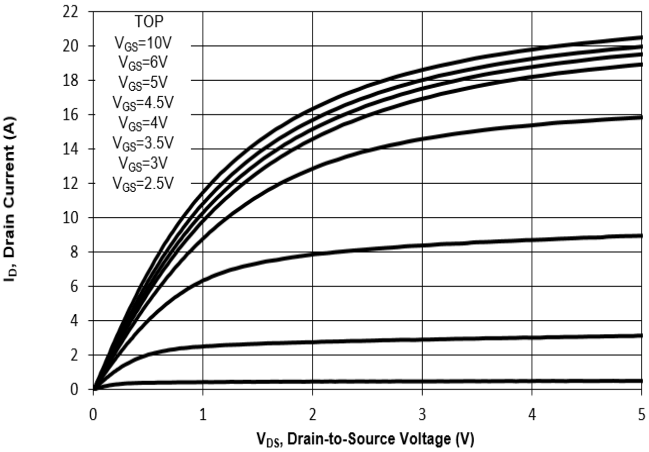


Fig. 2 Typical Transfer Characteristics

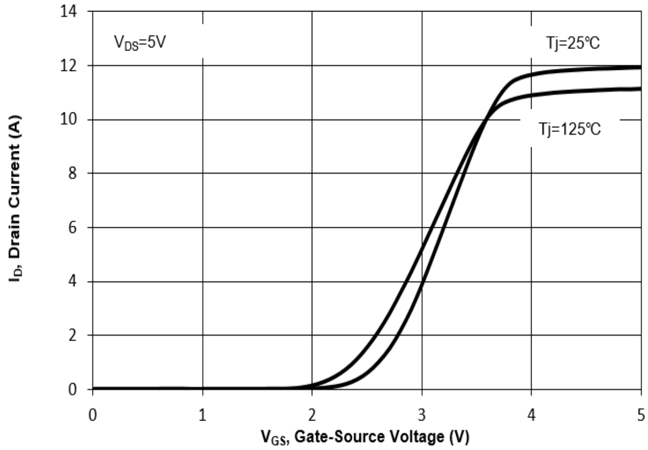


Fig. 3 on-Resistance vs. Drain Current

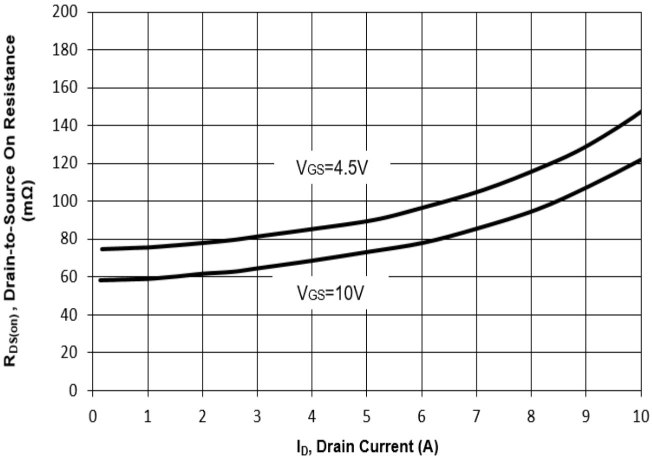


Fig. 4 on-Resistance vs. Gate to Source Voltage

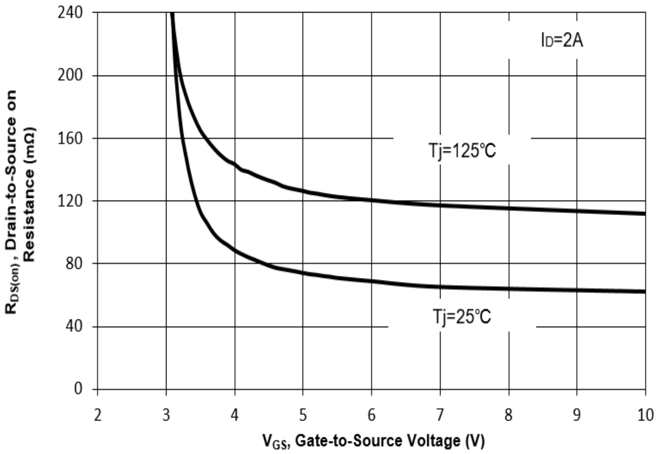


Fig. 5 on-Resistance vs.T_j

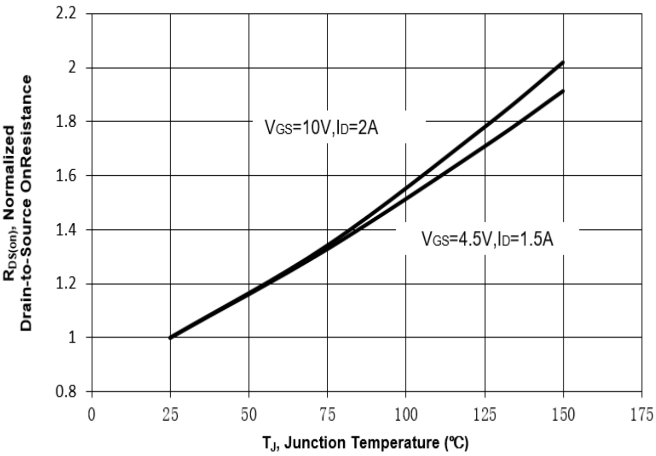
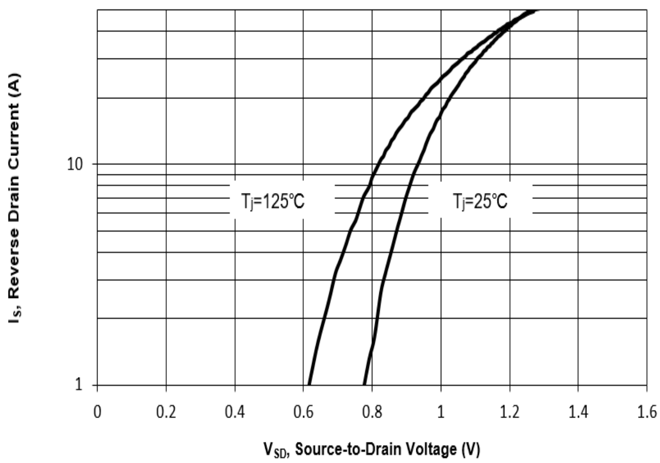


Fig. 6 Typical Body-Diode Forward Characteristics



Electrical Characteristics Curves

Fig. 7 Typical Junction Capacitance

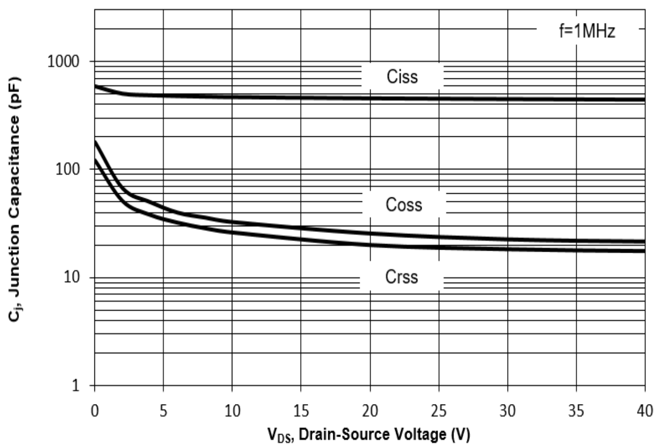


Fig. 8 Drain-Source Leakage Current vs. T_j

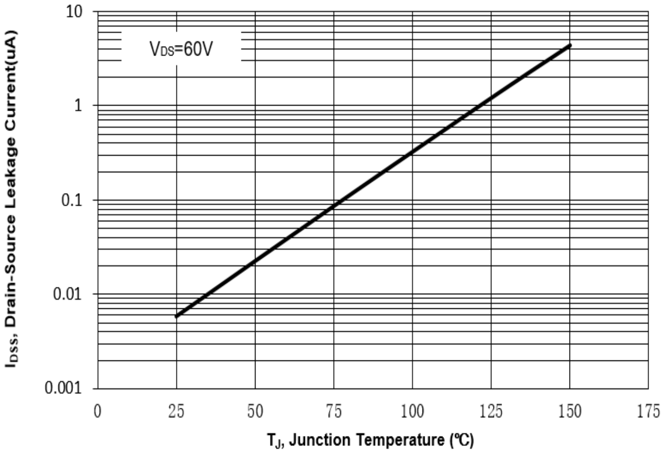


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

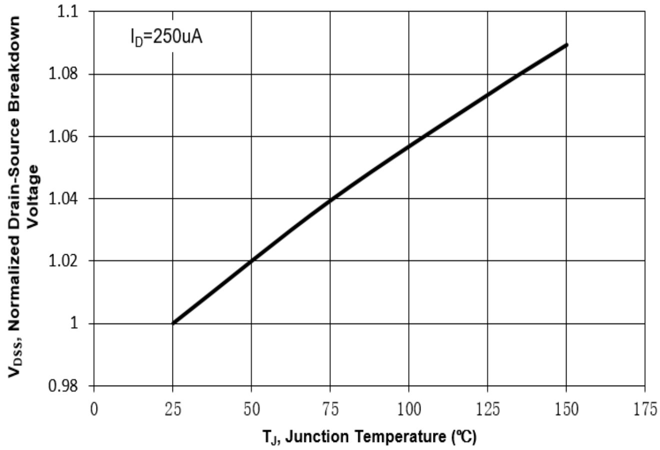


Fig. 10 Gate Threshold Variation vs. T_j

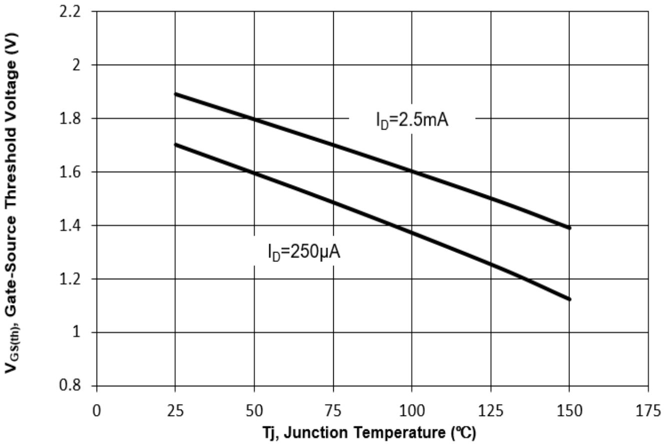


Fig. 11 Gate Charge

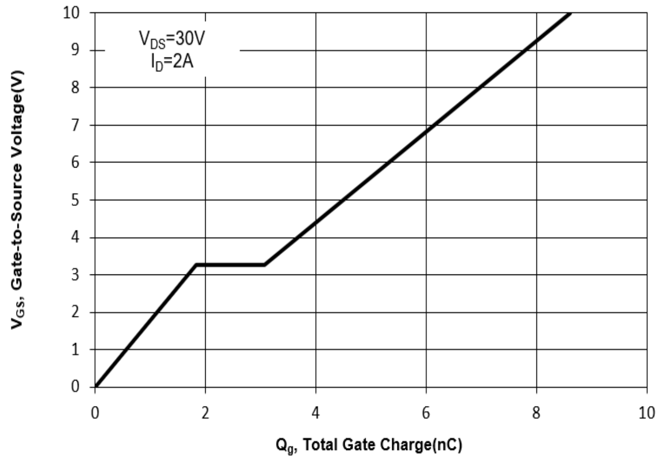
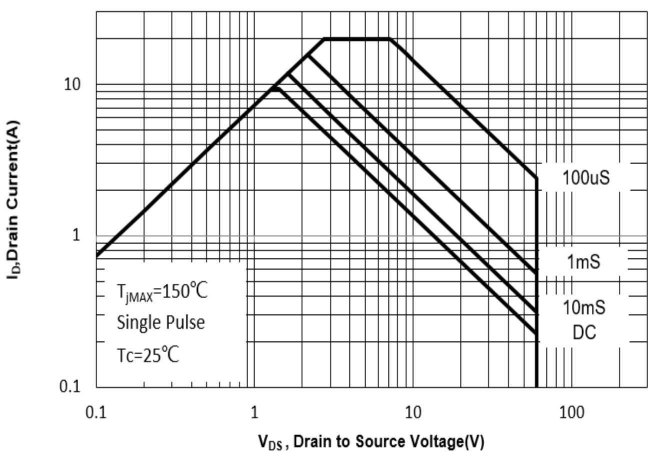


Fig. 12 Safe Operation Area



Electrical Characteristics Curves

Fig. 13 Normalized Maximum Transient Thermal Impedance($z_{\Theta JC}$)

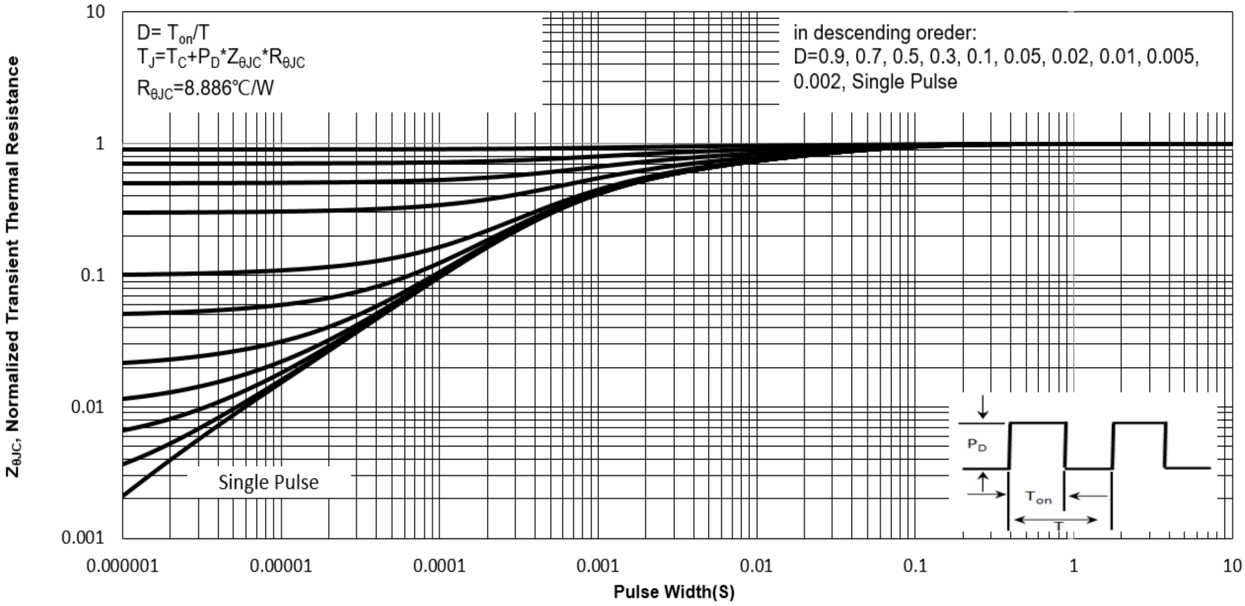
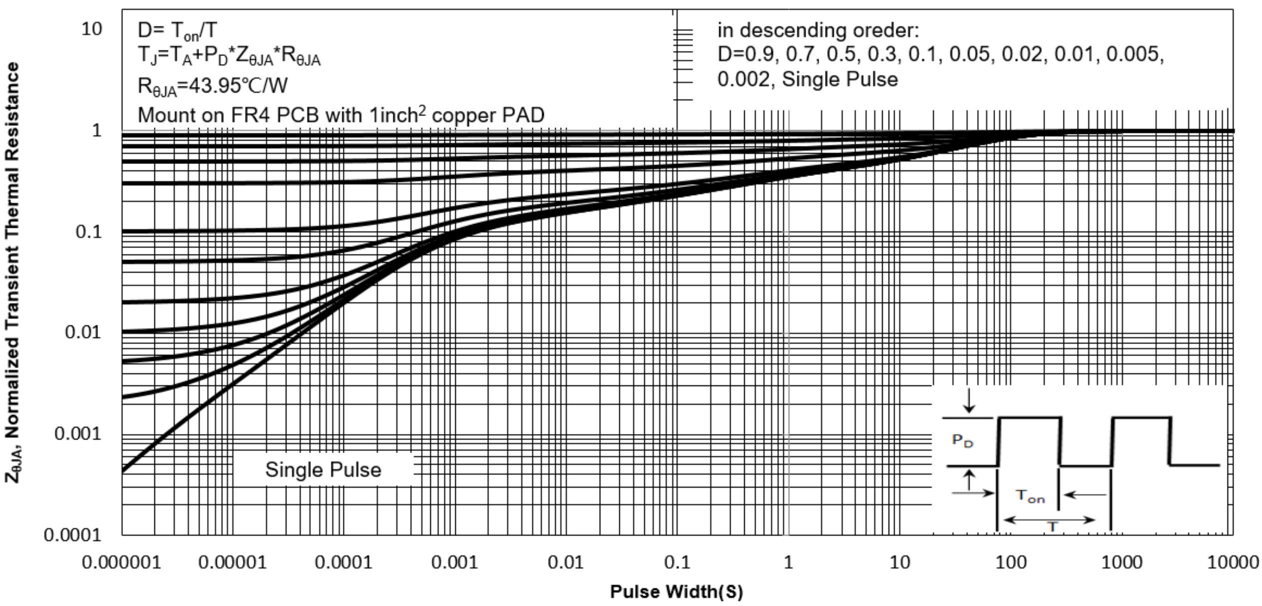


Fig. 14 Normalized Maximum Transient Thermal Impedance($z_{\Theta JA}$)



Test Circuits

Fig.1-1 Switching times test circuit

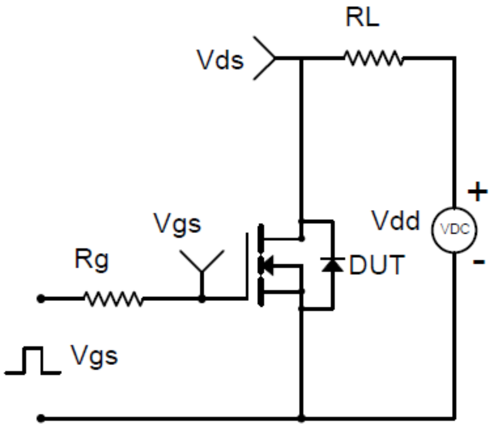


Fig.1-2 Switching Waveform

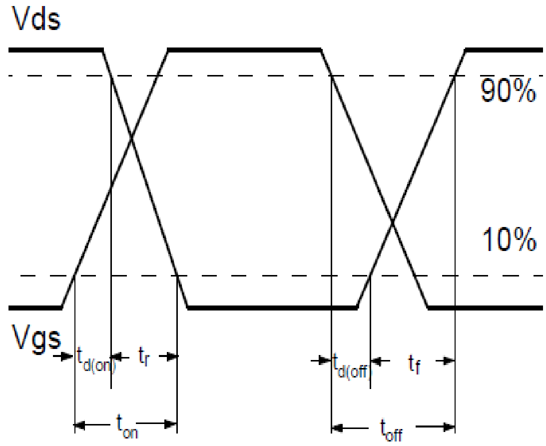


Fig.2-1 Gate charge test circuit

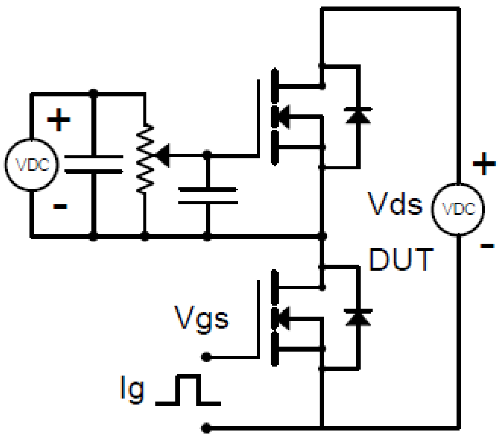


Fig.2-2 Gate charge waveform

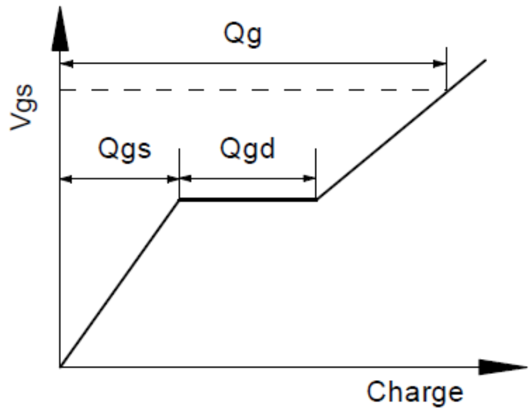


Fig.3-1 Avalanche test circuit

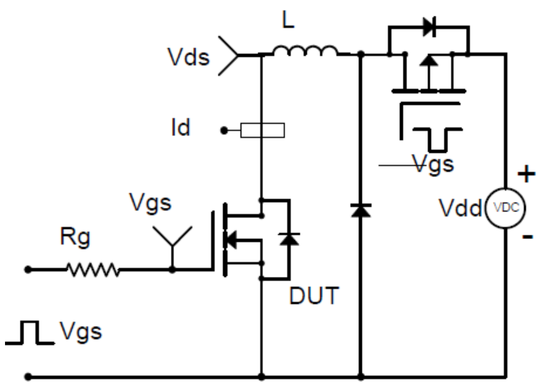
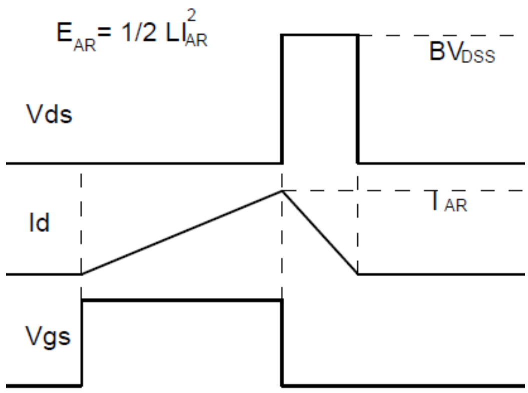
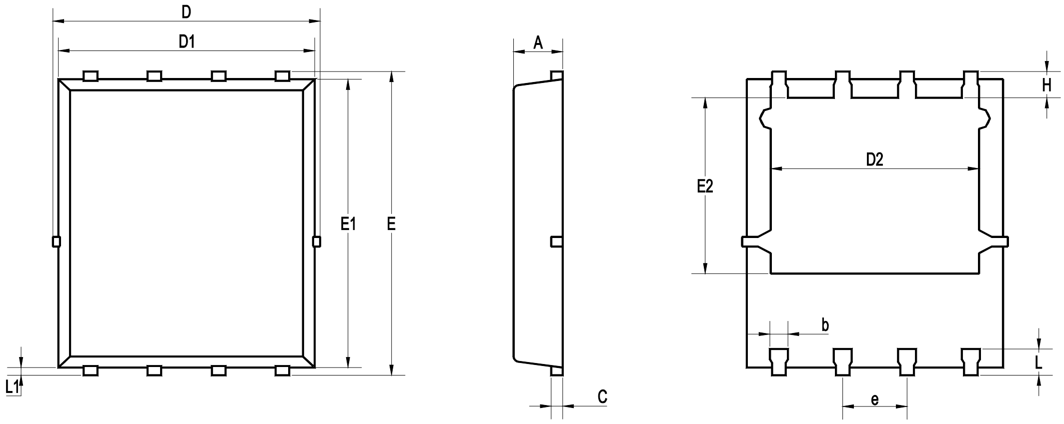


Fig.3-2 Avalanche waveform



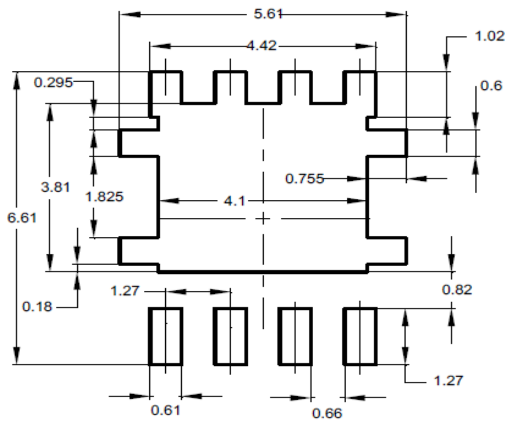
Package Outline Dimensions (Units: mm)

DFN5060



UNIT	A	b	C	D	D1	D2	E	E1	E2	e	L	L1	H
mm	1.12 0.9	0.51 0.33	0.34 0.11	5.26 4.7	5.1 4.7	4.5 3.56	6.25 5.75	6 5.6	3.66 3.18	1.37 1.17	0.71 0.35	0.2 0.06	0.71 0.35

Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
DFN5060	12	8 ± 0.1	0.315 ± 0.004	330	13	5,000

Marking information

" TM506N750LS " = Part No.
" ****** " = Date Code Marking
Font type: Arial