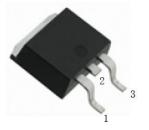
## WPR65N640-HAF

#### **N-Channel Enhancement Mode MOSFET**

#### **Features**

- Low R<sub>DS(on)</sub>
- Low Gate Charge
- Halogen and Antimony Free(HAF), RoHS compliant

# Gate Source



1.Gate 2.Drain 3.Source TO-252 Plastic Package

## **Application**

- DC-DC converters
- Lighting

**Key Parameters** 

Parameter	Value	Unit		
BV <sub>DSS</sub>	650	V		
R <sub>DS(ON)</sub> Max	0.64 @ V <sub>GS</sub> = 10 V	Ω		
V <sub>GS(th)</sub> typ	3	V		
Q <sub>g</sub> typ	10 @ V <sub>GS</sub> = 10 V	nC		

## Absolute Maximum Ratings(at Ta = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit	
Drain-Source Voltage	V <sub>DS</sub>	650	V	
Gate-Source Voltage	V <sub>G</sub> s	V <sub>GS</sub> ± 30		
Drain Current $ T_c = 25^{\circ}C $ $ T_c = 100^{\circ}C $	I <sub>D</sub>	6.4 4	А	
Peak Drain Current, Pulsed 1)	І <sub>ОМ</sub>	20	Α	
Avalanche Current	las	2.1	Α	
Single Pulse Avalanche Energy <sup>2)</sup>	E <sub>AS</sub>	174	mJ	
Power Dissipation T <sub>c</sub> = 25°C	PD	61.4	W	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to + 150	°C	

#### **Thermal Characteristics**

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	Rejc	2	°C/W
Thermal Resistance from Junction to Ambient 3)	R <sub>θJA</sub>	35	°C/W

<sup>&</sup>lt;sup>1)</sup> Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 2%, Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}$  = 150°C.



 $<sup>^{2)}</sup>$  Limited by  $T_{J(MAX)},$  starting  $T_J$  = 25 °C, L = 79 mH,  $R_g$  = 25  $\Omega,\,I_{AS}$  = 2.1 A,  $V_{GS}$  = 10 V.

<sup>&</sup>lt;sup>3)</sup> Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

# WPR65N640-HAF

Characteristics at Ta = 25°C unless otherwise specified

Parameter	Symbol	Min.	Тур.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I <sub>D</sub> = 250 μA	BV <sub>DSS</sub>	650	-	-	V
Drain-Source Leakage Current at V <sub>DS</sub> = 520 V	I <sub>DSS</sub>	-	-	1	μΑ
Gate Leakage Current at V <sub>GS</sub> = ± 24 V	I <sub>GSS</sub>	-	-	± 100	nA
Gate-Source Threshold Voltage at $V_{DS}$ = $V_{GS}$ , $I_D$ = 250 $\mu$ A	V <sub>GS(th)</sub>	2	-	4	V
Drain-Source On-State Resistance at $V_{GS} = 10 \text{ V}$ , $I_D = 3.5 \text{ A}$	R <sub>DS(on)</sub>	-	0.55	0.64	Ω
DYNAMIC PARAMETERS					
Forward Transconductance at $V_{DS}$ = 5 V, $I_D$ = 3.5 A	<b>g</b> FS	-	4.2	-	S
Gate Resistance at $V_{GS} = 0 \text{ V}$ , $V_{DS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$	Rg	-	5.8	-	Ω
Input Capacitance at $V_{GS} = 0 \text{ V}$ , $V_{DS} = 300 \text{ V}$ , $f = 1 \text{ MHz}$	C <sub>iss</sub>	-	399	-	pF
Output Capacitance at $V_{GS} = 0 \text{ V}$ , $V_{DS} = 300 \text{ V}$ , $f = 1 \text{ MHz}$	Coss	-	25	-	pF
Reverse Transfer Capacitance at $V_{GS} = 0 \text{ V}$ , $V_{DS} = 300 \text{ V}$ , $f = 1 \text{ MHz}$	C <sub>rss</sub>	-	4.9	-	pF
Gate charge total at $V_{DS}$ = 325 V, $V_{GS}$ = 10 V, $I_D$ = 3.5 A	Qg	-	10	-	nC
Gate to Source Charge at $V_{DS}$ = 325 V, $V_{GS}$ = 10 V, $I_D$ = 3.5 A	Q <sub>gs</sub>	-	2.7	-	nC
Gate to Drain Charge at $V_{DS}$ = 325 V, $V_{GS}$ = 10 V, $I_D$ = 3.5 A	$Q_{gd}$	-	3.6	-	nC
Turn-On Delay Time at $V_{DS}$ = 325 V, $V_{GS}$ = 10 V, $I_D$ = 3.5 A, $R_G$ = 24 $\Omega$	t <sub>d(on)</sub>	-	22	-	ns
Turn-On Rise Time at $V_{DS}$ = 325 V, $V_{GS}$ = 10 V, $I_D$ = 3.5 A, $R_G$ = 24 $\Omega$	t <sub>r</sub>	-	14	-	ns
Turn-Off Delay Time at $V_{DS}$ = 325 V, $V_{GS}$ = 10 V, $I_D$ = 3.5 A, $R_G$ = 24 $\Omega$	$t_{\text{d(off)}}$	-	17	-	ns
Turn-Off Fall Time at $V_{DS}$ = 325 V, $V_{GS}$ = 10 V, $I_D$ = 3.5 A, $R_G$ = 24 $\Omega$	t <sub>f</sub>	-	51	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I <sub>S</sub> = 1 A, V <sub>GS</sub> = 0 V	V <sub>SD</sub>	-	-	1.4	V
Body-Diode Continuous Current	Is	-	-	6.4	Α
Body-Diode Continuous Current, Pulsed	Іѕм	-	-	20	Α
Body Diode Reverse Recovery Time at I <sub>S</sub> = 3.5 A, di/dt = 100 A / μs	t <sub>rr</sub>	-	275	-	ns
Body Diode Reverse Recovery Charge at I <sub>s</sub> = 3.5 A, di/dt = 100 A / µs	Qrr	-	1.5	-	μC



#### **Electrical Characteristics Curves**

Fig. 1 Typical Output Characteristics

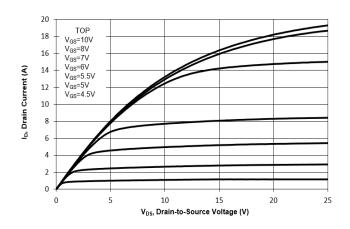


Fig. 2 Typical Transfer Characteristics

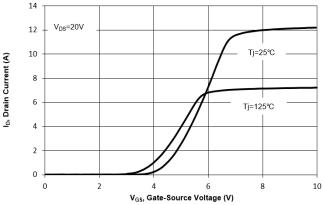


Fig. 3 On-Resistance vs. Drain Current

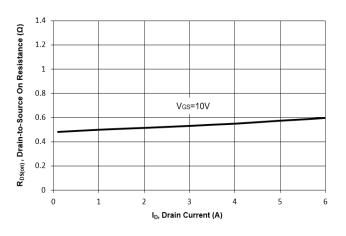


Fig. 4 On-Resistance vs. Gate to Source Voltage

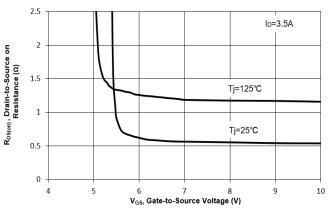


Fig. 5 On-Resistance vs.T<sub>j</sub>

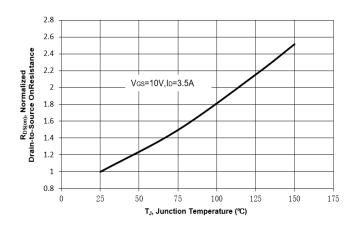
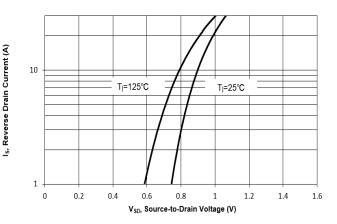


Fig. 6 Typical Body-Diode Forward Characteristics





#### **Electrical Characteristics Curves**

Fig. 7 Typical Junction Capacitance

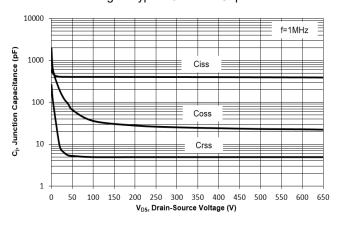


Fig. 8 Drain-Source Leakage Current vs. Tj

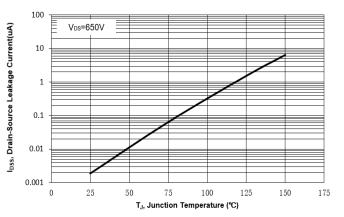


Fig. 9  $V_{(BR)DSS}$  vs. Junction Temperature

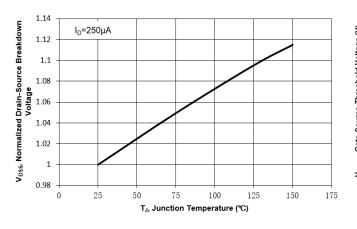


Fig. 10 Gate Threshold Variation vs. T<sub>j</sub>

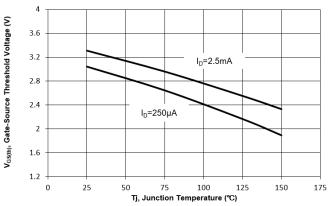


Fig. 11 Gate Charge

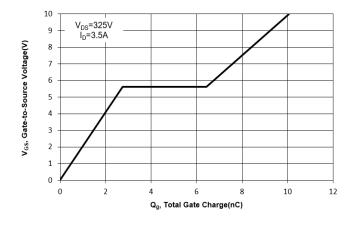
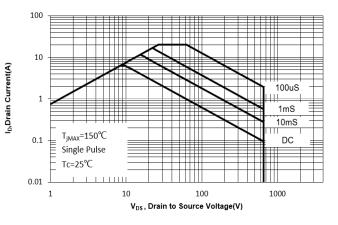


Fig. 12 Safe Operation Area





## **Electrical Characteristics Curves**

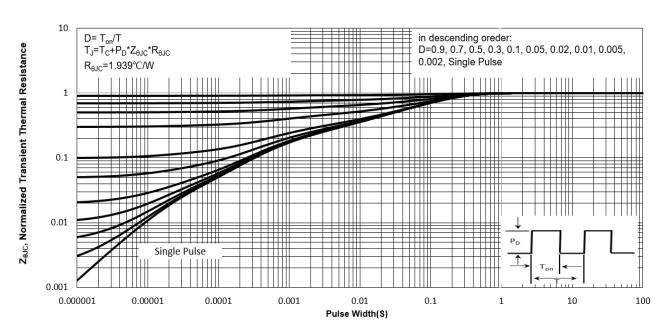
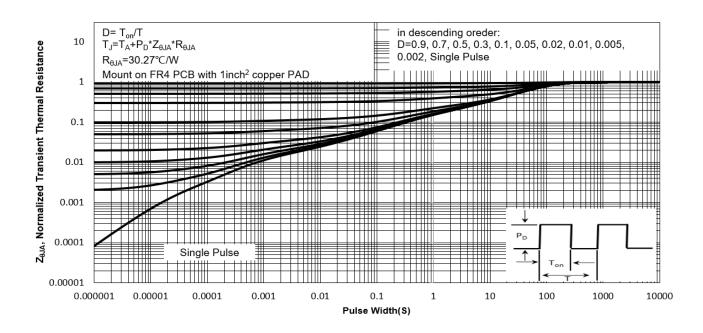


Fig.13 Normalized Maximum Transient Thermal Impedance(zeuc)

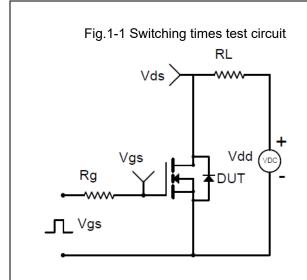






# WPR65N640-HAF

## **Test Circuits**



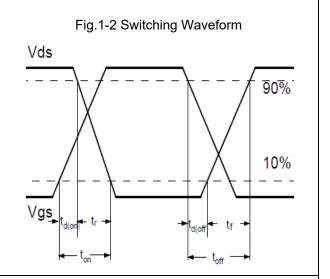


Fig.2-1 Gate charge test circuit

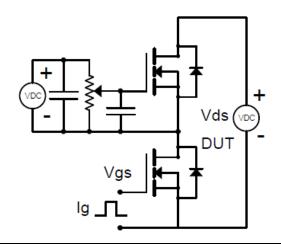


Fig.2-2 Gate charge waveform

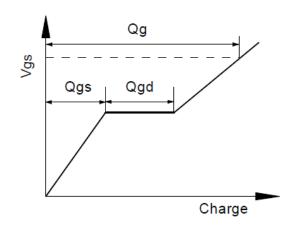


Fig.3-1 Avalanche test circuit

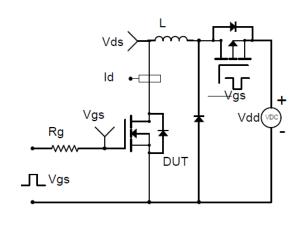
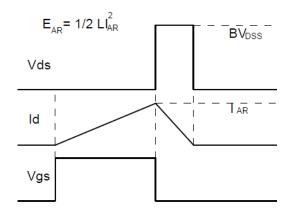


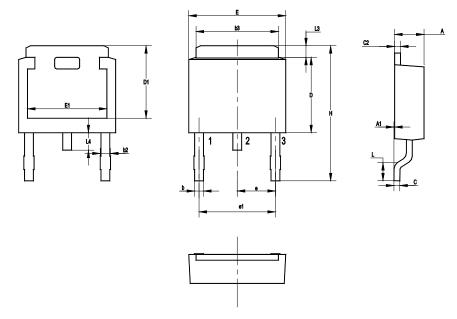
Fig.3-2 Avalanche waveform





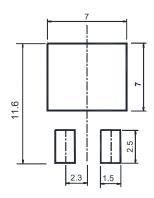
# Package Outline (Dimensions in mm)

TO-252



UNIT	Α	A1	b	b2	b3	С	C2	D	D1	Е	E1	е	e1	Н	L	L3	L4
	2.5	0.15	1.0	1.15	5.5	0.65	0.65	6.2	5.4	6.7	5.0	2.30	4.60	10.7	1.78	1.20	1.10
mm	2.1	0	0.5	0.65	4.9	0.4	0.4	5.6	5.0	6.1	4.6	TYP.	TYP.	9	1.40	0.85	0.51

## **Recommended Soldering Footprint**



Packing information

· uoking iiiio							
Package	Tape Width	Pit	tch	Reel	Size	Per Reel Packing Quantity	
Fackage	(mm)	mm	inch	mm	inch	rei Neel Fackling Quantity	
TO-252	16	8 ± 0.1	0.315 ± 0.004	330	13	2,500	

## **Marking information**

- " PR65N640 " = Part No.
- " \*\*\*\*\* " = Date Code Marking

Font type: Arial



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