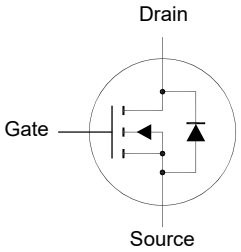
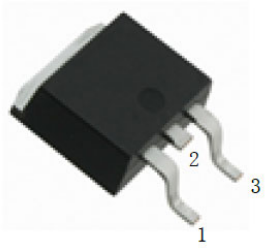
WDR10N170LS-HAF

N-Channel Enhancement Mode MOSFET

Features

- Low $R_{DS(ON)}$
- Fully Characterized Capacitance and Avalanche
- Halogen and Antimony Free(HAF), RoHS compliant





1.Gate 2.Drain 3.Source
TO-252 Plastic Package

Application

- Synchronous Rectification
- BLDC Motor drive applications
- Battery powered circuits

Key Parameters

Parameter	Value	Unit
BV_{DSS}	100	V
$R_{DS(ON)}$ Max	17 @ V_{GS} = 10 V	mΩ
	23 @ V_{GS} = 4.5 V	
$V_{GS(th)}$ typ	2	V
Q_g typ	22 @ V_{GS} = 10 V	nC

Absolute Maximum Ratings (at T_a = 25℃ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	T_c = 25℃ T_c = 100℃	I_D	44 30	A
Peak Drain Current, Pulsed [1]		I_{DM}	140	A
Avalanche Current		I_{AS}	17.4	A
Single Pulse Avalanche Energy [2]		E_{AS}	15	mJ
Drain-Source Voltage, Spike (tp = 10 μs)		V_{SPIKE}	120	V
Power Dissipation	T_c = 25℃ T_a = 25℃	P_{tot}	62.5 3	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	℃

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2.4	℃/W
Thermal Resistance from Junction to Ambient [3]	$R_{\theta JA}$	50	℃/W

[1] Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 2%, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ = 175°C.

[2] Limited by $T_{J(MAX)}$, starting T_J = 25 °C, L = 0.1 mH, R_g = 25 Ω, I_{AS} = 17.4 A, V_{GS} = 10 V.

[3] Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

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Characteristics at T_a = 25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I_D = 1 mA	BV_{DSS}	100	-	-	V
Drain-Source Leakage Current at V_{DS} = 100 V	I_{DSS}	-	-	1	μA
Gate Leakage Current at V_{GS} = ± 20 V	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at V_{DS} = V_{GS}, I_D = 250 μA	$V_{GS(th)}$	1.2	-	2.5	V
Drain-Source On-State Resistance at V_{GS} = 10 V, I_D = 7 A at V_{GS} = 4.5 V, I_D = 5 A	$R_{DS(on)}$	- -	14 18.7	17 23	mΩ
DYNAMIC PARAMETERS					
Forward Transconductance at V_{DS} = 5 V, I_D = 7 A	g_{fs}	-	16	-	S
Gate resistance at V_{GS} = 0 V, V_{DS} = 0 V, f = 1 MHz	R_g	-	0.6	-	Ω
Input Capacitance at V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz	C_{iss}	-	1093	-	pF
Output Capacitance at V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz	C_{oss}	-	538	-	pF
Reverse Transfer Capacitance at V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz	C_{rss}	-	69	-	pF
Gate charge total at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 7 A at V_{DS} = 50 V, V_{GS} = 4.5 V, I_D = 7 A	Q_g	- -	22 12	- -	nC
Gate to Source Charge at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 7 A	Q_{gs}	-	3	-	nC
Gate to Drain Charge at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 7 A	Q_{gd}	-	6	-	nC
Turn-On Delay Time at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 7 A, R_g = 4.7 Ω	$t_{d(on)}$	-	14	-	ns
Turn-On Rise Time at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 7 A, R_g = 4.7 Ω	t_r	-	8	-	ns
Turn-Off Delay Time at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 7 A, R_g = 4.7 Ω	$t_{d(off)}$	-	14	-	ns
Turn-Off Fall Time at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 7 A, R_g = 4.7 Ω	t_f	-	5	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I_S = 1 A, V_{GS} = 0 V	V_{SD}	-	-	1	V
Body-Diode Continuous Current	I_S	-	-	44	A
Body-Diode Continuous Current, Pulsed	I_{SM}	-	-	140	A
Body Diode Reverse Recovery Time at I_S = 7 A, di/dt = 100 A / μs	t_{rr}	-	37	-	ns
Body Diode Reverse Recovery Charge at I_S = 7 A, di/dt = 100 A / μs	Q_{rr}	-	32	-	nC

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

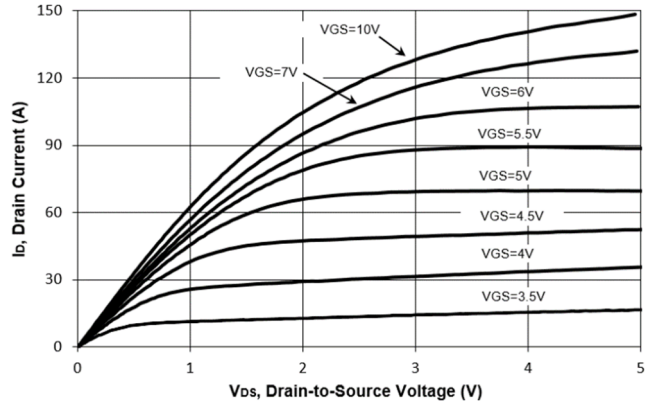


Fig. 2 Typical Transfer Characteristics

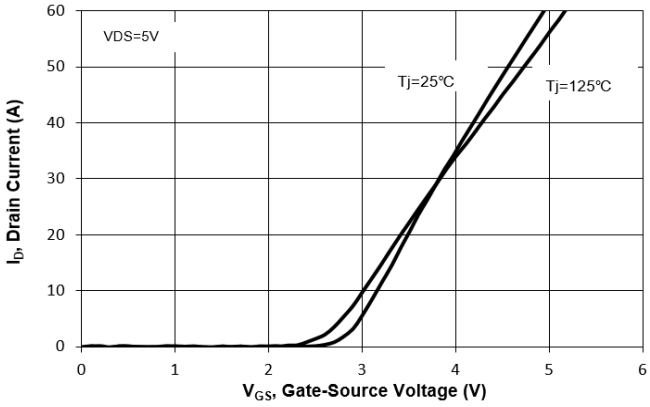


Fig. 3 On-Resistance vs. Drain Current

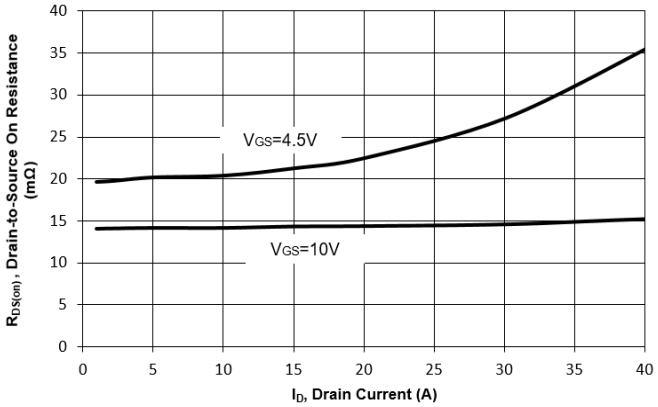


Fig. 4 on-Resistance vs. Gate to Source Voltage

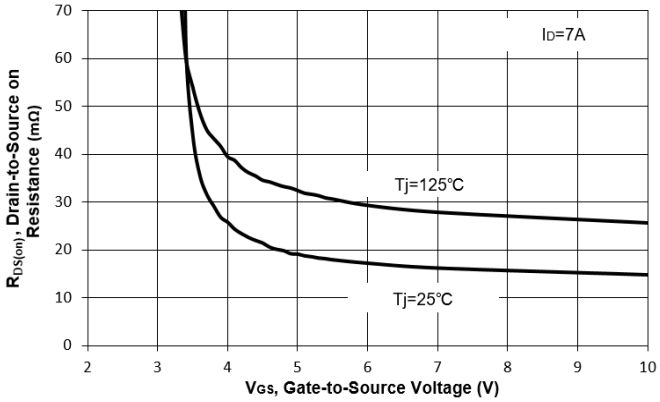


Fig. 5 on-Resistance vs.T_j

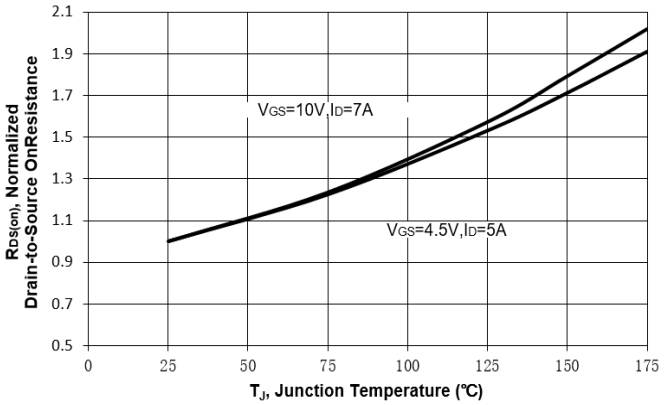
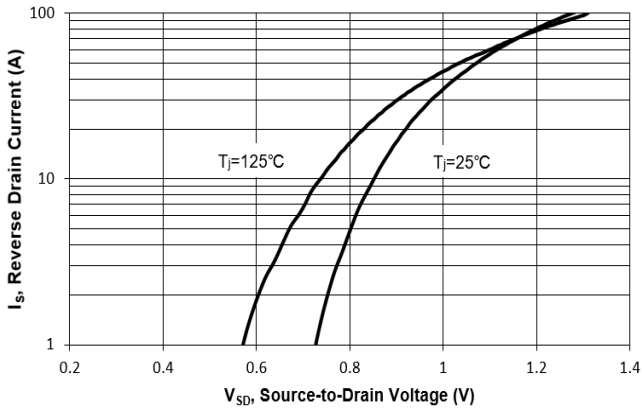


Fig. 6 Typical Body-Diode Forward Characteristics



Electrical Characteristics Curves

Fig. 7 Typical Junction Capacitance

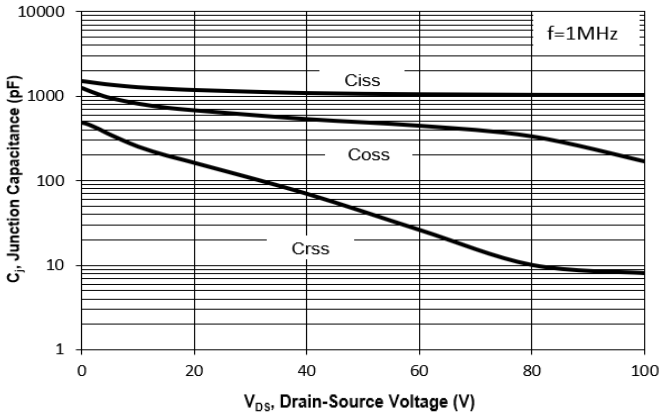


Fig. 8 Drain-Source Leakage Current vs. T_j

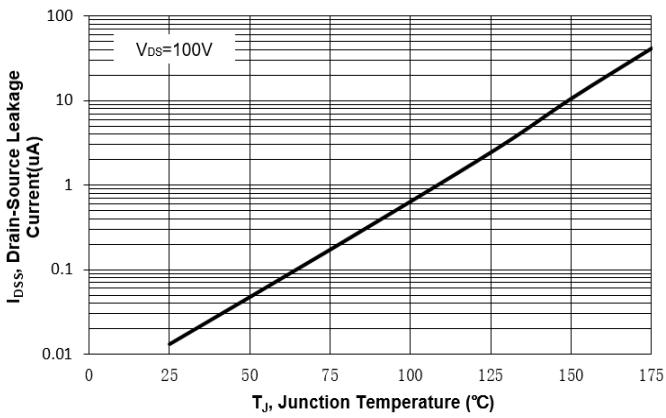


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

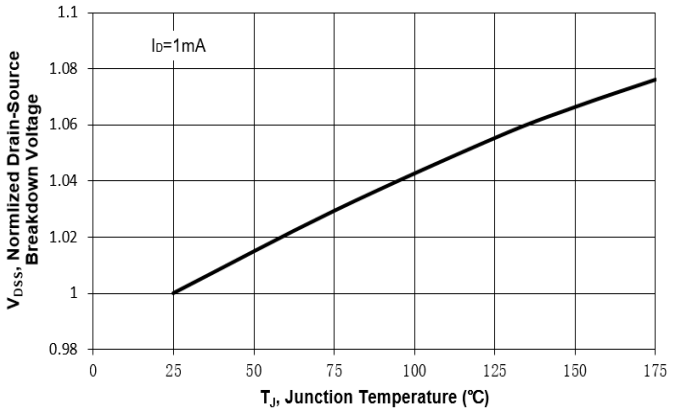


Fig. 10 Gate Threshold Variation vs. T_j

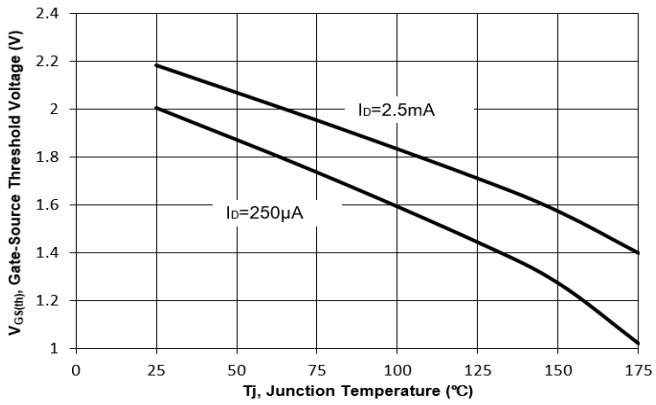


Fig. 11 Gate Charge

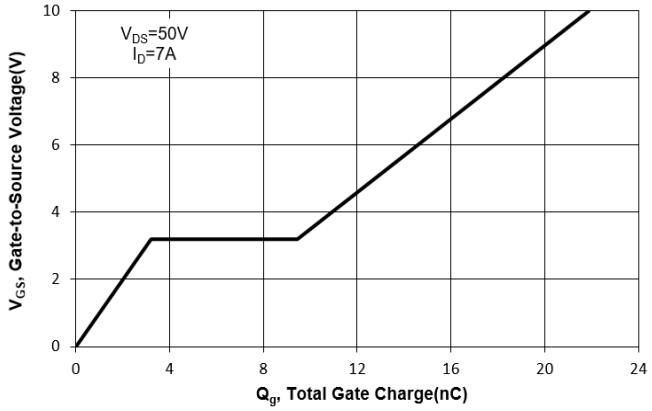
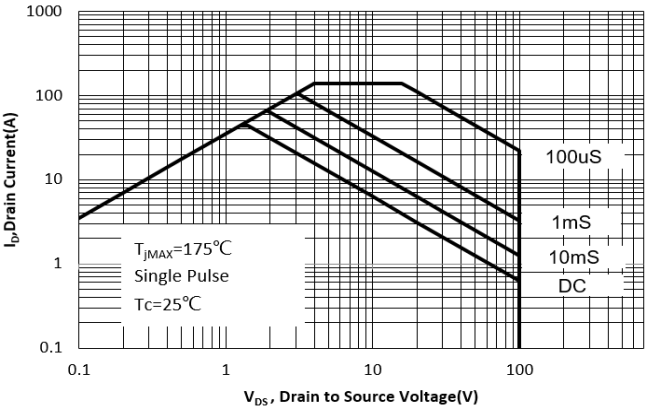


Fig.12 SOA,Safe Operating Area



Electrical Characteristics Curves

Fig. 13 Normalized Maximum Transient Thermal Impedance($z_{\Theta JC}$)

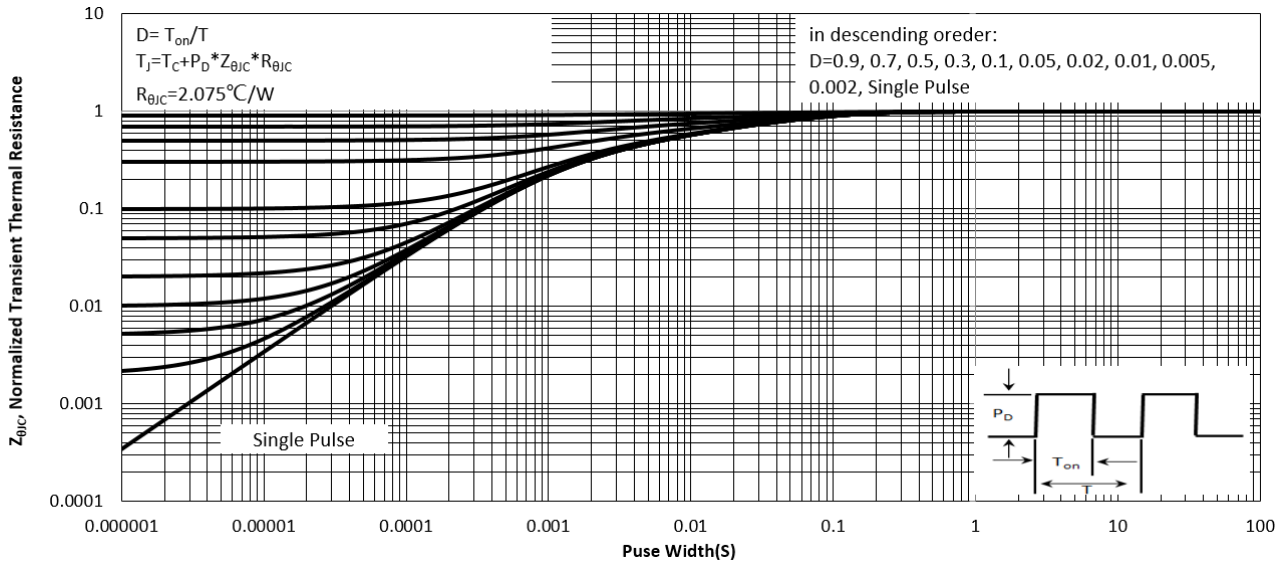
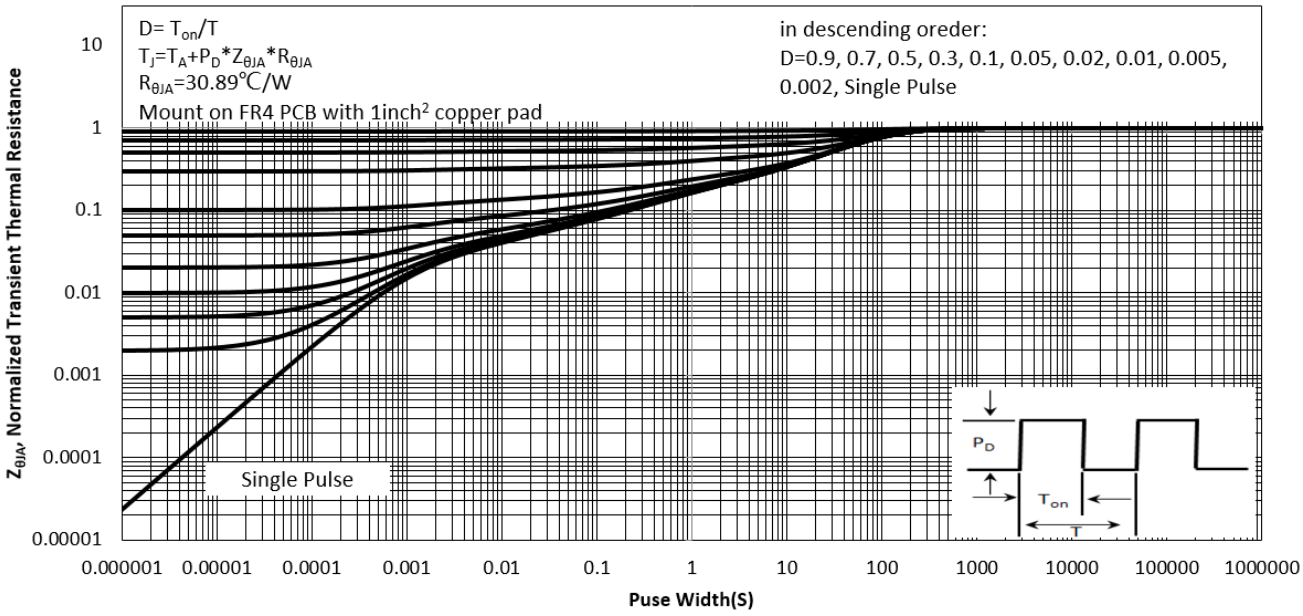


Fig. 14 Normalized Maximum Transient Thermal Impedance($z_{\Theta JA}$)



Test Circuits

Fig.1-1 Switching times test circuit

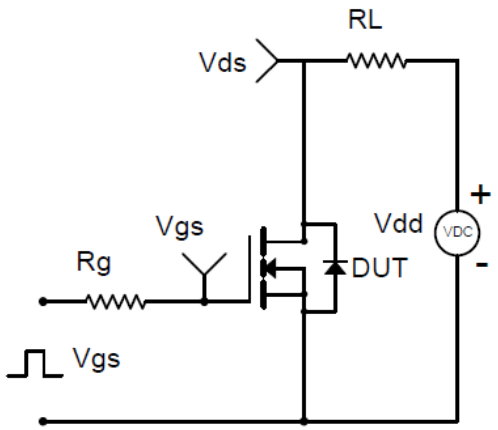


Fig.1-2 Switching Waveform

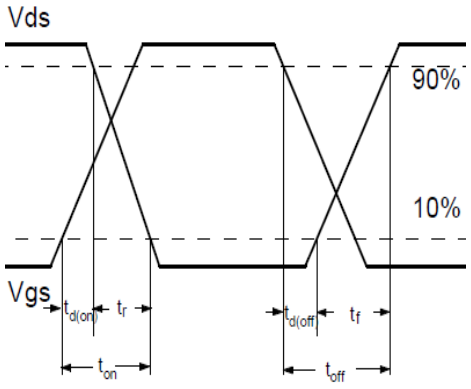


Fig.2-1 Gate charge test circuit

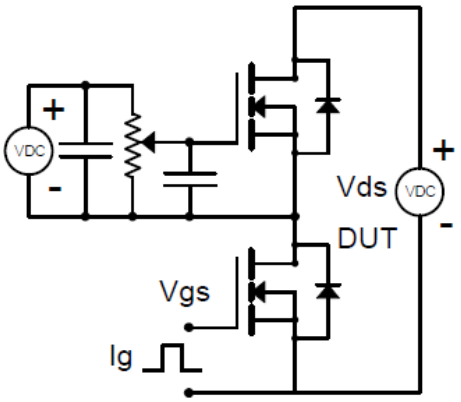


Fig.2-2 Gate charge waveform

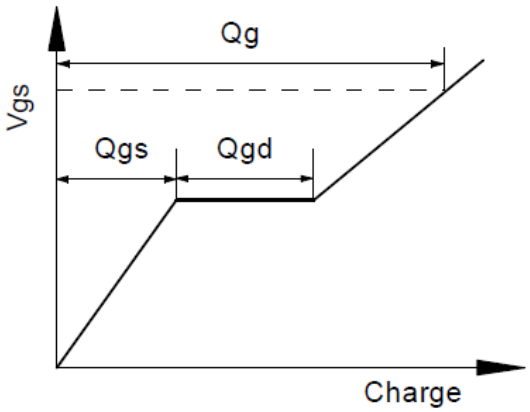


Fig.3-1 Avalanche test circuit

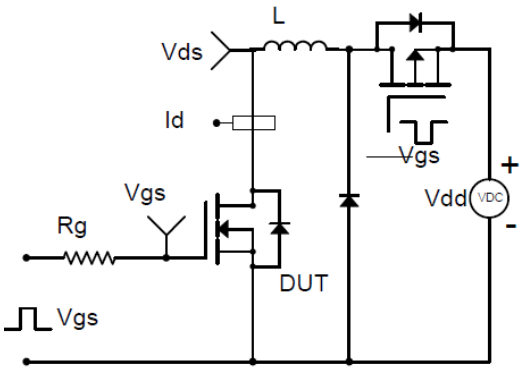
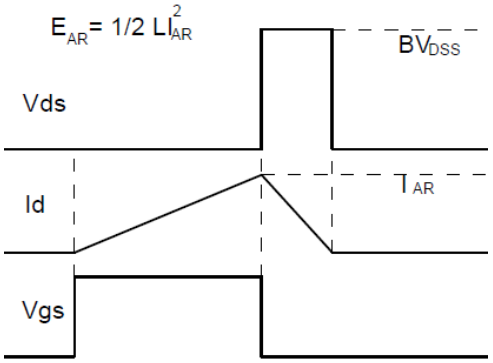
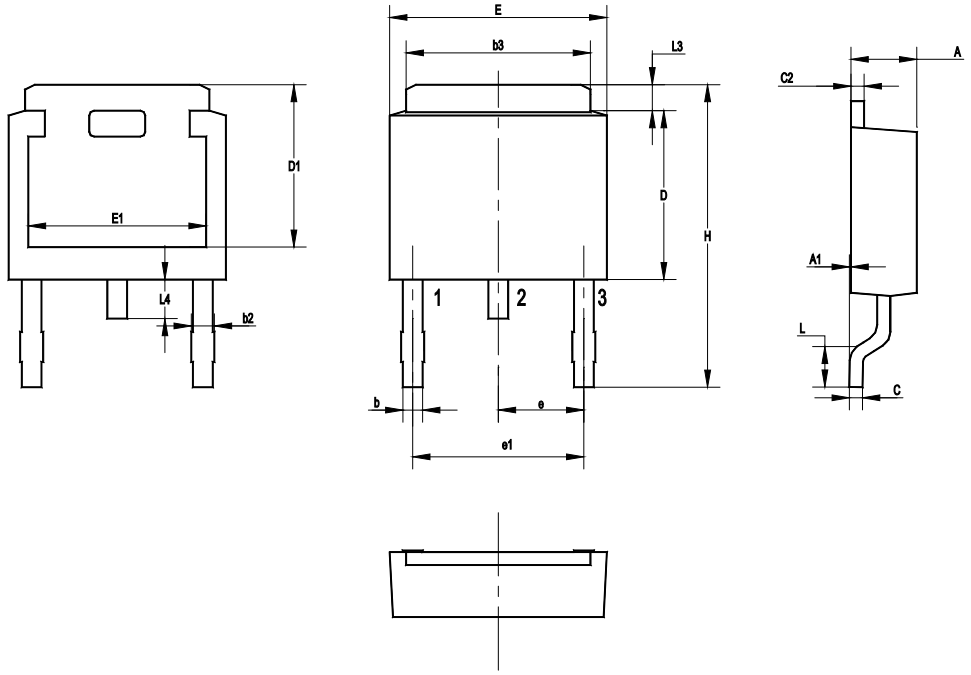


Fig.3-2 Avalanche waveform

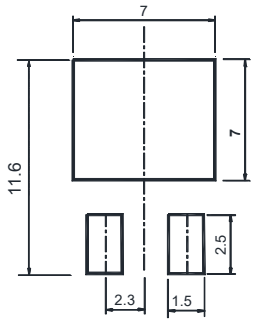


Package Outline (Dimensions in mm) TO-252



UNIT	A	A1	b	b2	b3	C	C2	D	D1	E	E1	e	e1	H	L	L3	L4
mm	2.5	0.15	1.0	1.15	5.5	0.65	0.65	6.2	5.4	6.7	5.0	2.30	4.60	10.7	1.78	1.20	1.10
	2.1	0	0.5	0.65	4.9	0.4	0.4	5.6	5.0	6.1	4.6	TYP.	TYP.	9	1.40	0.85	0.51

Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
TO-252	16	8 ± 0.1	0.315 ± 0.004	330	13	2,500

Marking information

" DR10N170LS " = Part No.

" ****** " = Date Code Marking

Font type: Arial

Dated: 24/10/2023 Rev: 06