

MU10N160L-CH

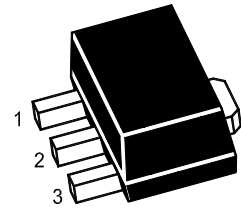
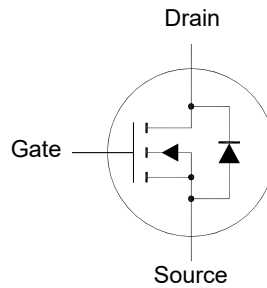
N-Channel Enhancement Mode MOSFET

Features

- AEC-Q101 Qualified
- Extremely low threshold voltage
- Halogen and Antimony Free(HAF),
RoHS compliant

Applications

- Portable appliances
- Battery management
- High speed switch



1.Gate 2.Drain 3.Source
SOT-89 Plastic Package

Absolute Maximum Ratings (at $T_a = 25^\circ\text{C}$ unless otherwise specified)

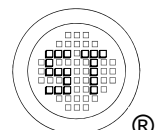
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current	I_D	6 3	A
Peak Drain Current, Pulsed ¹⁾	I_{DM}	20	A
Total Power Dissipation ²⁾	P_{tot}	2	W
Operating Junction and Storage Temperature Range	T_j, T_{stg}	- 55 to + 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Ambient ²⁾	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Thermal Resistance from Junction to Case	$R_{\theta JC}$	13	$^\circ\text{C/W}$

¹⁾ Pulse width $\leq 10 \mu\text{s}$, duty cycle $\leq 1\%$.

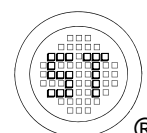
²⁾ Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.



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Characteristics at $T_a = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at $I_D = 250 \mu\text{A}$	$V_{(BR)DSS}$	100	-	-	V
Zero Gate Voltage Drain Current at $V_{DS} = 80 \text{ V}$	I_{DSS}	-	-	1	μA
Gate-Source Leakage at $V_{GS} = \pm 16 \text{ V}$	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at $V_{DS} = V_{DS}, I_D = 250 \mu\text{A}$	$V_{GS(th)}$	1.3	-	2.5	V
Drain-Source On-State Resistance at $V_{GS} = 10 \text{ V}, I_D = 6 \text{ A}$ at $V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$	$R_{DS(on)}$	- -	- -	150 160	m Ω
DYNAMIC PARAMETERS					
Forward Transconductance at $V_{DS} = 5 \text{ V}, I_D = 4 \text{ A}$	g_{Fs}	-	9.8	-	S
Gate Resistance at $V_{DS} = 0 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	R_g	-	1.1	-	Ω
Input Capacitance at $V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	C_{iss}	-	1155	-	pF
Output Capacitance at $V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	C_{oss}	-	28	-	pF
Reverse Transfer Capacitance at $V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	C_{rss}	-	25	-	pF
Gate Charge Total at $V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}$ at $V_{DS} = 50 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$	Q_g	- -	20 9	- -	nC
Gate to Source Charge at $V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}$	Q_{gs}	-	4	-	nC
Gate to Drain Charge at $V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}$	Q_{gd}	-	2.4	-	nC
Turn-On Delay Time at $V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}, R_g = 3.3 \Omega$	$t_{d(on)}$	-	14	-	ns
Turn-On Rise Time at $V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}, R_g = 3.3 \Omega$	t_r	-	4	-	ns
Turn-Off Delay Time at $V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}, R_g = 3.3 \Omega$	$t_{d(off)}$	-	13	-	ns
Turn-Off Fall Time at $V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4 \text{ A}, R_g = 3.3 \Omega$	t_f	-	2	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at $V_{GS} = 0 \text{ V}, I_S = 1 \text{ A}$	V_{SD}	-	-	1.3	V
Body-Diode Continuous Current	I_S	-	-	3	A
Body Diode Reverse Recovery Time at $I_S = 4 \text{ A}, di/dt = 100 \text{ A} / \mu\text{s}$	t_{rr}	-	21	-	ns
Body Diode Reverse Recovery Charge at $I_S = 4 \text{ A}, di/dt = 100 \text{ A} / \mu\text{s}$	Q_{rr}	-	22	-	nC



Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

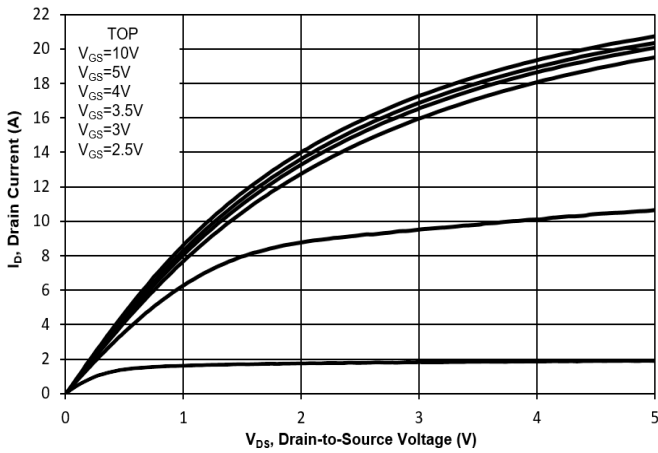


Fig. 2 Typical Transfer Characteristics

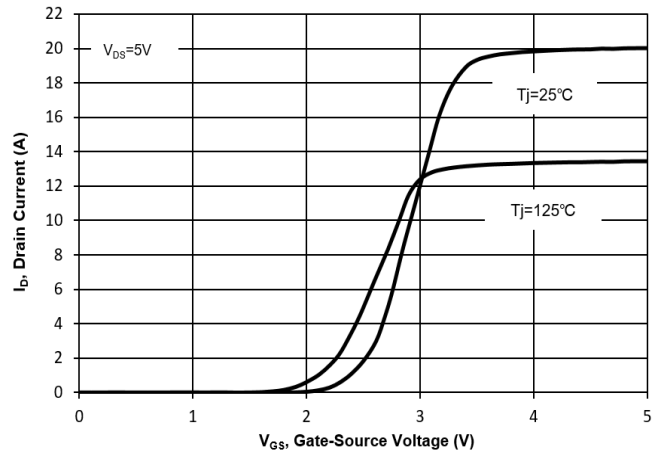


Fig. 3 On-Resistance vs. Drain Current

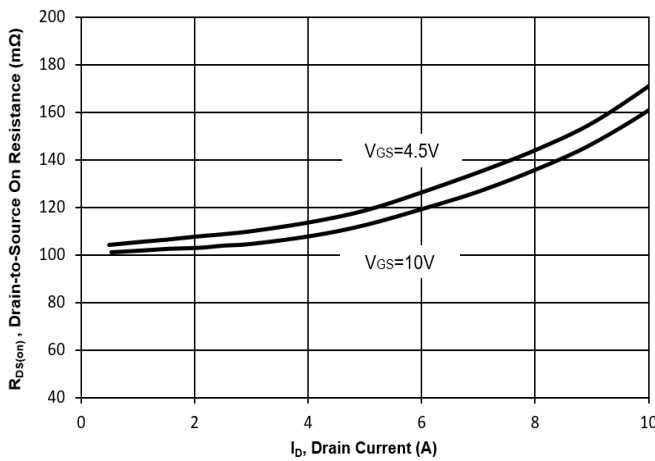


Fig. 4 On-Resistance vs. Gate-Source Voltage

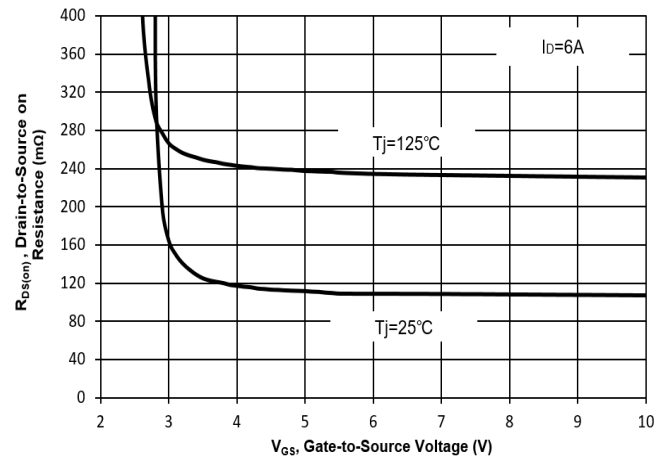


Fig. 5 On-Resistance vs. T_j

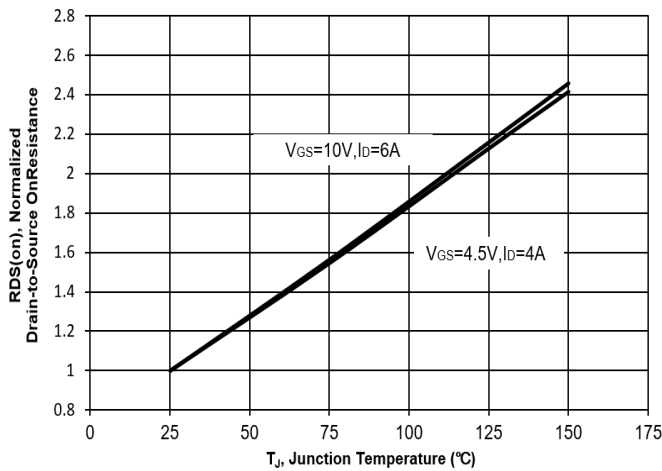
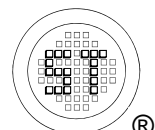
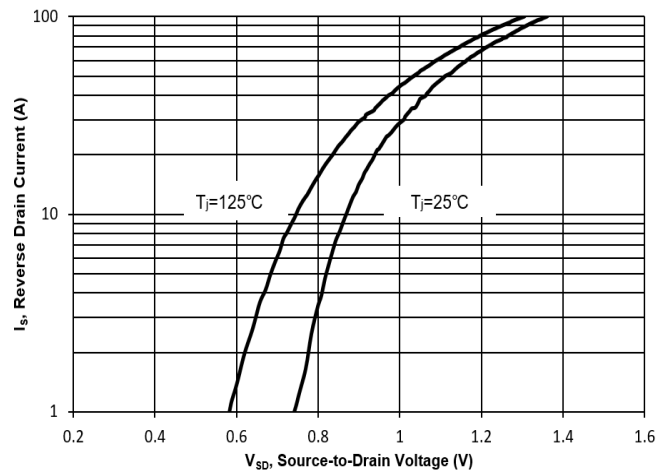


Fig. 6 Typical Body-Diode Forward Characteristics



Electrical Characteristics Curves

Fig. 7 Typical Junction Capacitance

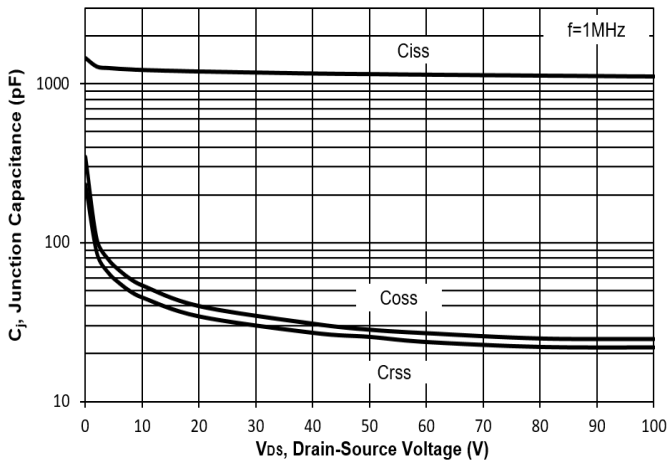


Fig. 8 Drain-Source Leakage Current vs. T_j

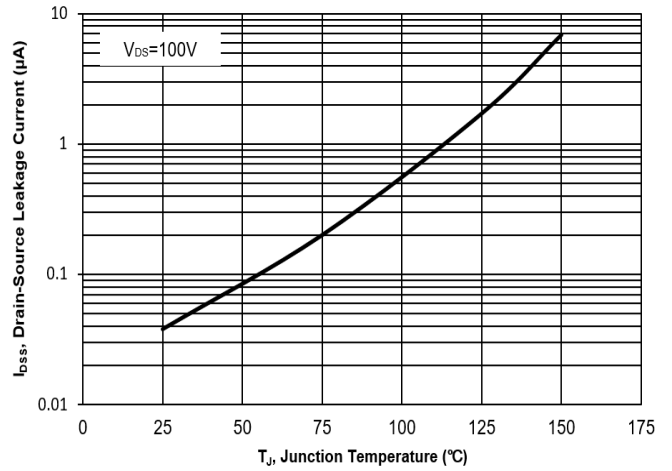


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

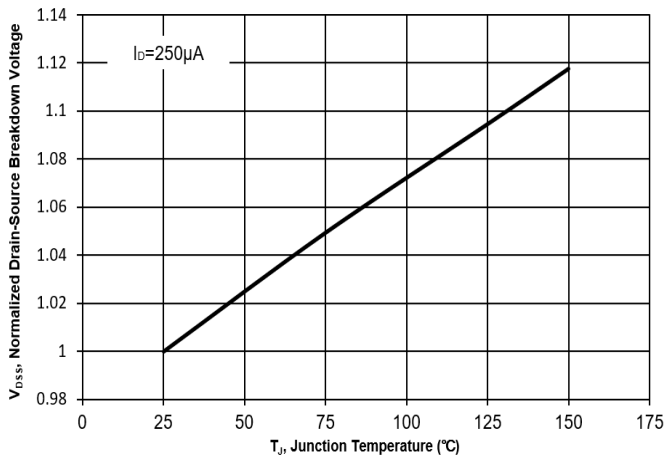


Fig. 10 Gate Threshold Variation vs. T_j

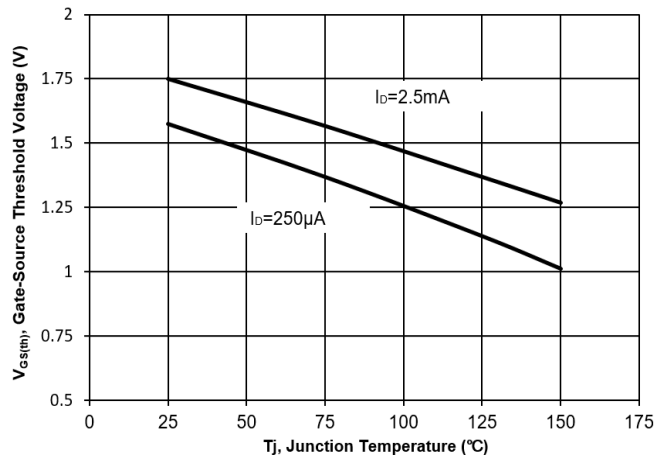
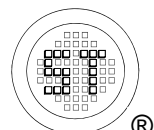
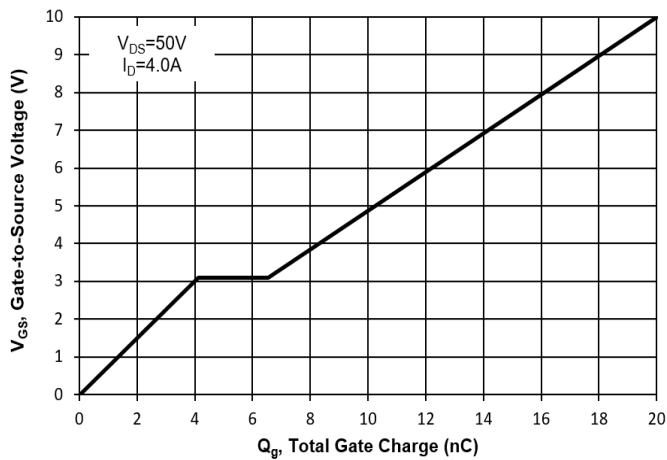


Fig. 11 Gate Charge



Test Circuits

Fig.1-1 Switching times test circuit

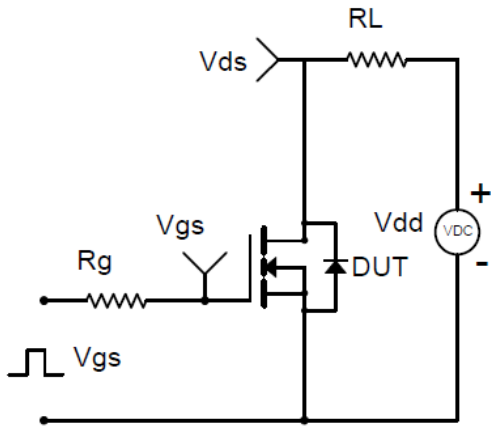


Fig.1-2 Switching Waveform

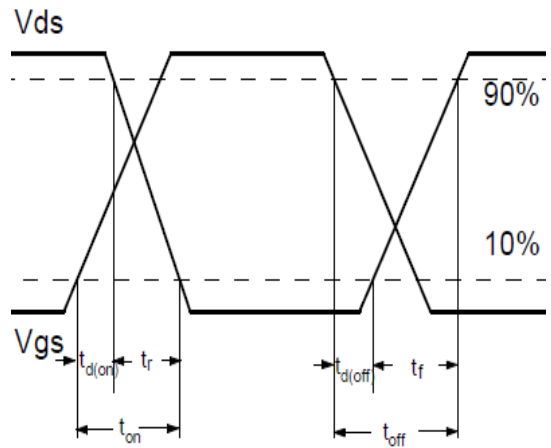


Fig.2-1 Gate charge test circuit

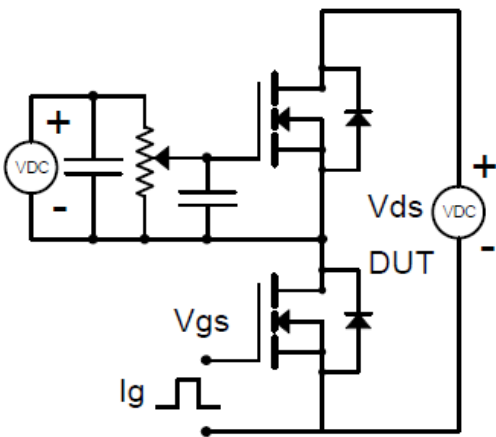
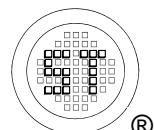
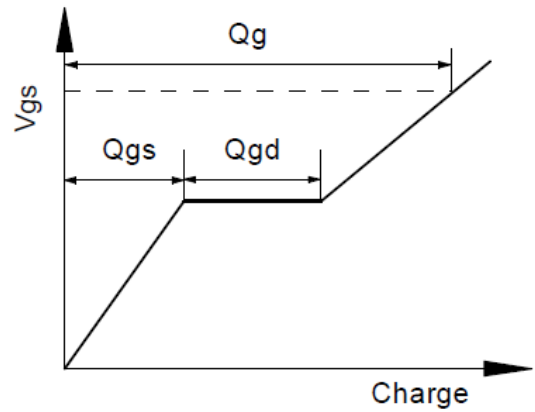


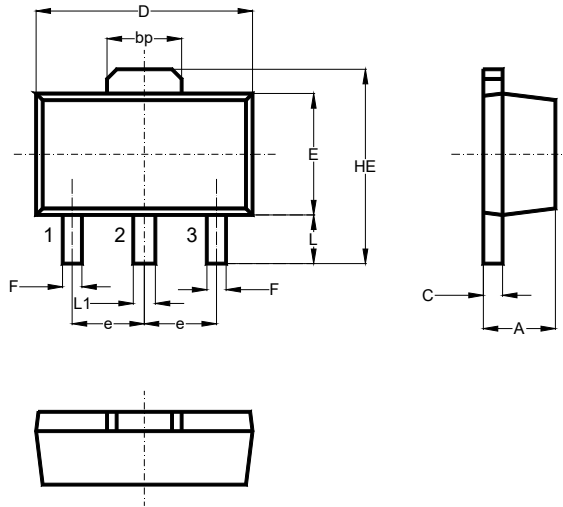
Fig.2-2 Gate charge waveform



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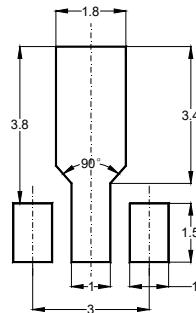
Package Outline (Dimensions in mm)

SOT-89



Unit	A	bp	C	D	E	F	HE	e	L	L1
mm	1.6	1.60	0.5	4.6	2.6	0.45	4.25	1.5	1.05	0.51
	1.4	1.50	0.3	4.4	2.4	0.35	3.75	typ.	0.95	0.41

Recommended Soldering Footprint



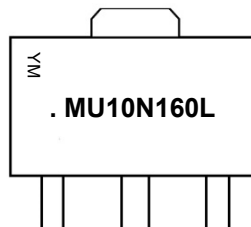
Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
SOT-89	12	8 ± 0.1	0.315 ± 0.004	178	7	1,000
				330	13	4,000

Marking information

- " MU10N160L " = Part No.
- " . " = HAF (Halogen and Antimony Free)
- " YM " = Date Code Marking
- " Y " = Year
- " M " = Month

Font type: Arial



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