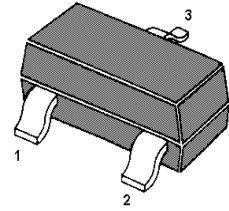
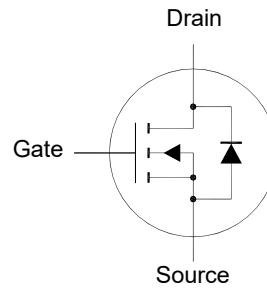


MKA10N560L

N-Channel Enhancement Mode MOSFET

Features

- Surface-mounted package



1. Gate 2. Source 3. Drain
SOT-23 Plastic Package

Applications

- Portable appliances
- Battery management

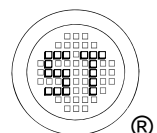
Absolute Maximum Ratings(at $T_a = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	1	A
Peak Drain Current, Pulsed	I_{DM}	4	A
Power Dissipation ¹⁾	P_D	1	W
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 55 to + 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Ambient ¹⁾	$R_{\theta JA}$	125	$^\circ\text{C}/\text{W}$

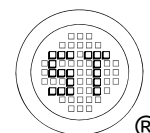
¹⁾ Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air, $t < 10$ s.



MKA10N560L

Characteristics at $T_a = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at $I_D = 1\text{ mA}$	BV_{DSS}	100	-	-	V
Drain-Source Leakage Current at $V_{DS} = 100\text{ V}$	I_{DSS}	-	-	1	μA
Gate Leakage Current at $V_{GS} = \pm 20\text{ V}$	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at $V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	$V_{GS(th)}$	1	-	2.5	V
Drain-Source On-State Resistance at $V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$ at $V_{GS} = 4.5\text{ V}$, $I_D = 1\text{ A}$ at $V_{GS} = 4\text{ V}$, $I_D = 1\text{ A}$	$R_{DS(on)}$	-	-	520 560 580	$\text{m}\Omega$
DYNAMIC PARAMETERS					
Forward Transconductance at $V_{DS} = 5\text{ V}$, $I_D = 1\text{ A}$	g_{Fs}	-	4.1	-	S
Gate resistance at $V_{DS} = 0\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	R_g	-	0.9	-	Ω
Input Capacitance at $V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$	C_{iss}	-	454	-	pF
Output Capacitance at $V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$	C_{oss}	-	17	-	pF
Reverse Transfer Capacitance at $V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$	C_{rss}	-	13	-	pF
Gate charge total at $V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$ at $V_{DS} = 50\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 1\text{ A}$	Q_g	-	8.4 3.9	-	nC
Gate-Source Charge at $V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$	Q_{gs}	-	1.9	-	nC
Gate-Drain Charge at $V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$	Q_{gd}	-	1.1	-	nC
Turn-On Delay Time at $V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$, $R_g = 3.3\ \Omega$	$t_{d(on)}$	-	9.5	-	nS
Turn-On Rise Time at $V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$, $R_g = 3.3\ \Omega$	t_r	-	4	-	nS
Turn-Off Delay Time at $V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$, $R_g = 3.3\ \Omega$	$t_{d(off)}$	-	8	-	nS
Turn-Off Fall Time at $V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 1\text{ A}$, $R_g = 3.3\ \Omega$	t_f	-	13	-	nS
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at $I_S = 1\text{ A}$, $V_{GS} = 0\text{ V}$	V_{SD}	-	-	1.2	V
Body-Diode Continuous Current	I_S	-	-	1	A
Body Diode Reverse Recovery Time at $I_S = 1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	t_{rr}	-	17	-	nS
Body Diode Reverse Recovery Charge at $I_S = 1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	Q_{rr}	-	14.5	-	nC



Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

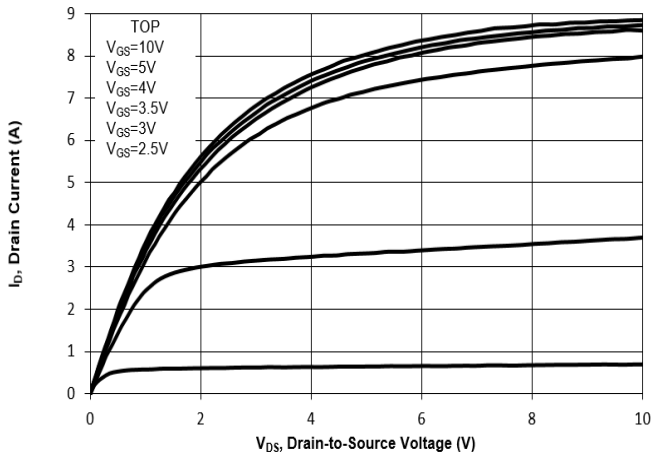


Fig. 2 Typical Transfer Characteristics

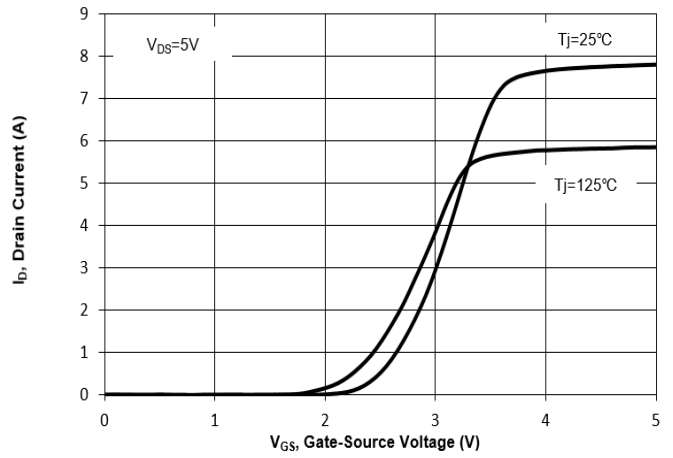


Fig. 3 On-Resistance vs. Drain Current

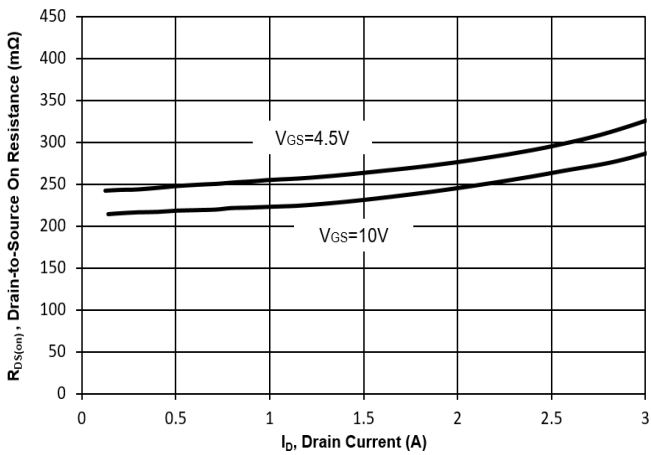


Fig. 4 On-Resistance vs. Gate-Source Voltage

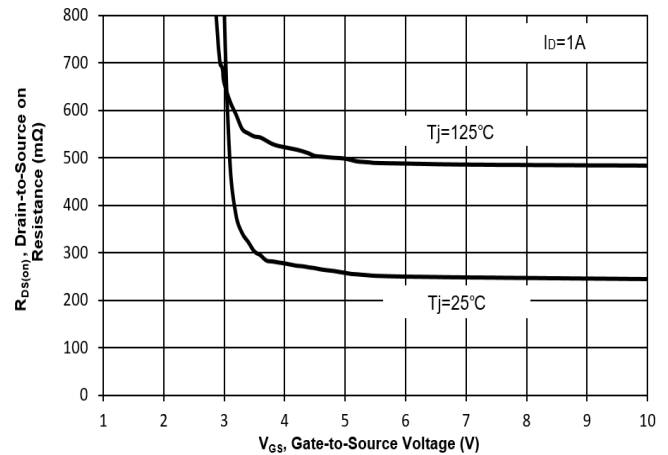


Fig. 5 On-Resistance vs. T_J

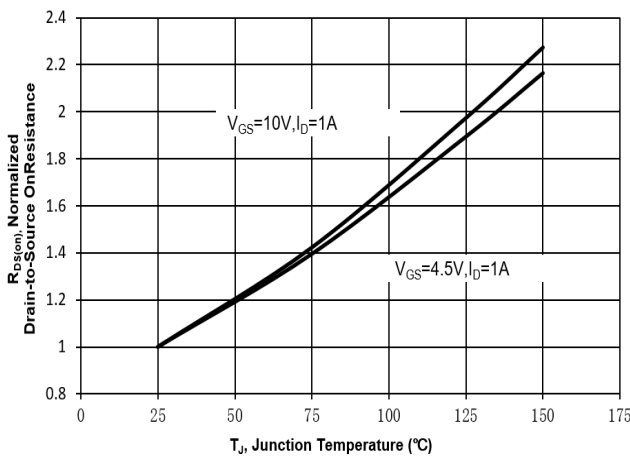
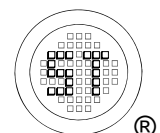
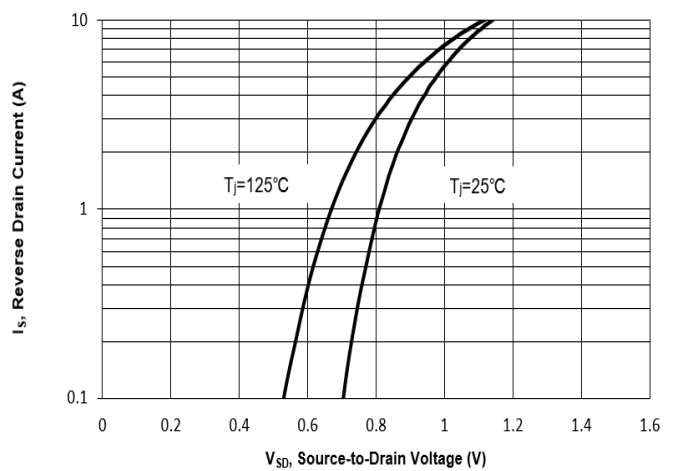


Fig. 6 Typical Body-Diode Forward Characteristics



Electrical Characteristics Curves

Fig. 7 Typical Junction Capacitance

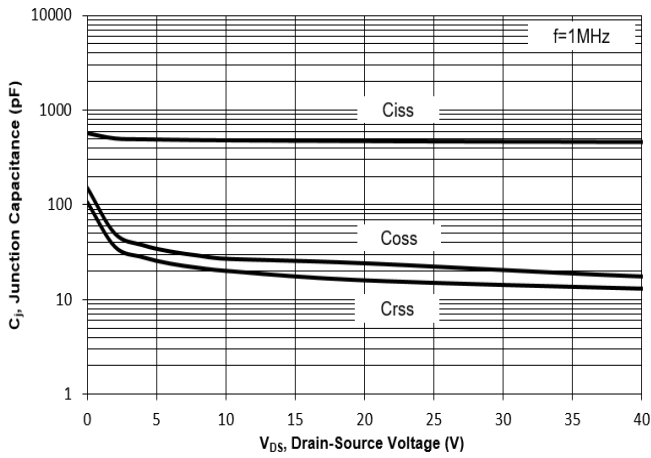


Fig. 8 Drain-Source Leakage Current vs. T_J

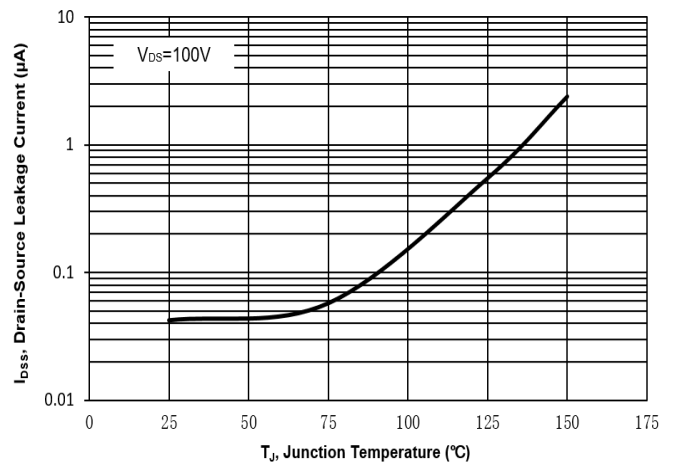


Fig. 9 V_{(BR)DSS} vs. Junction Temperature

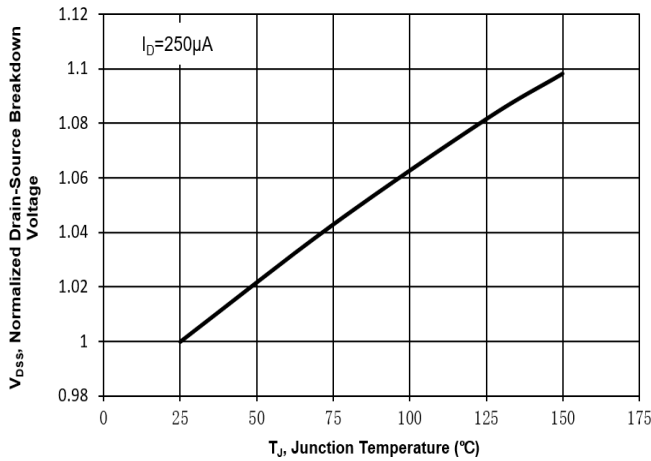


Fig. 10 Gate Threshold Variation vs. T_J

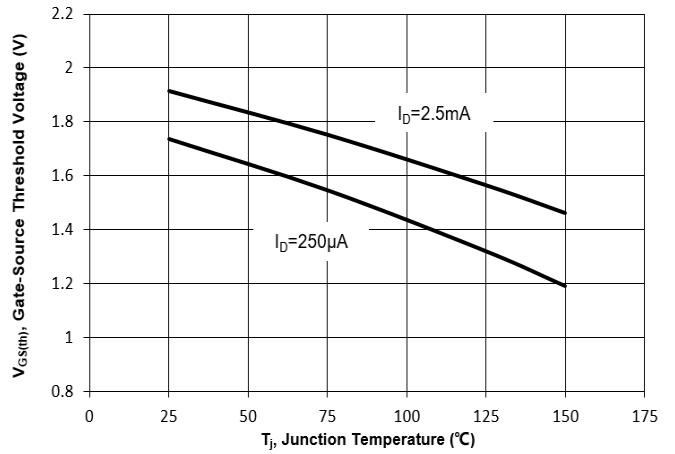
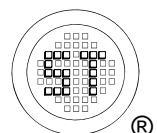
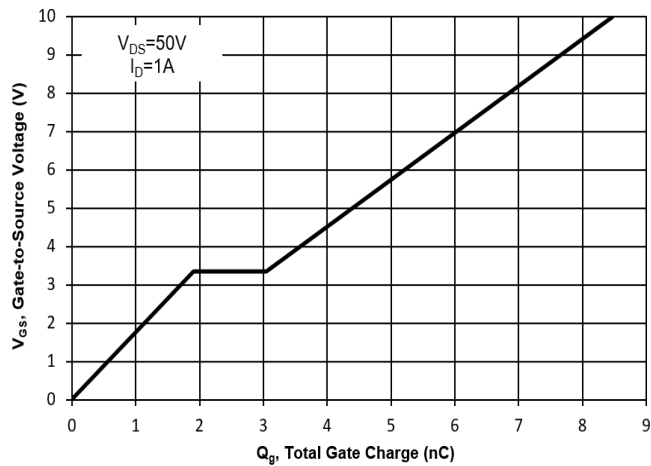


Fig. 11 Gate Charge



Test Circuits

Fig.1-1 Switching times test circuit

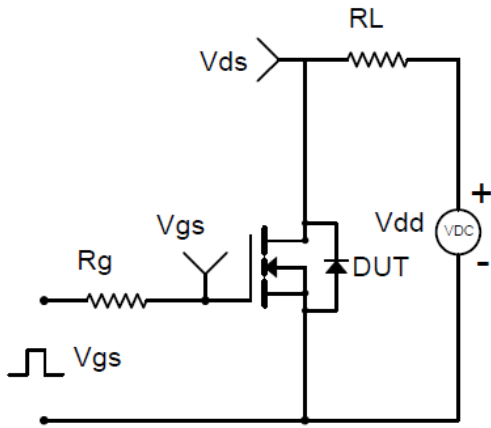


Fig.1-2 Switching Waveform

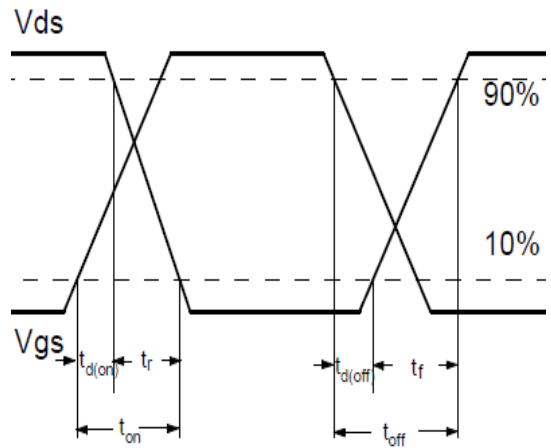


Fig.2-1 Gate charge test circuit

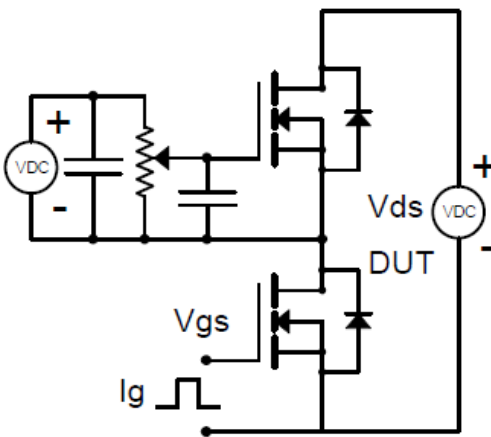
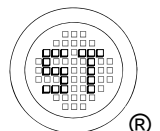
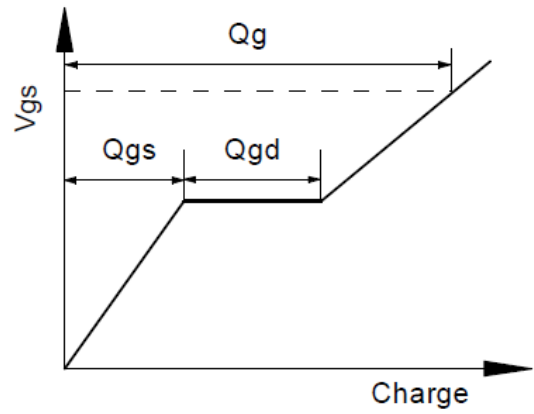


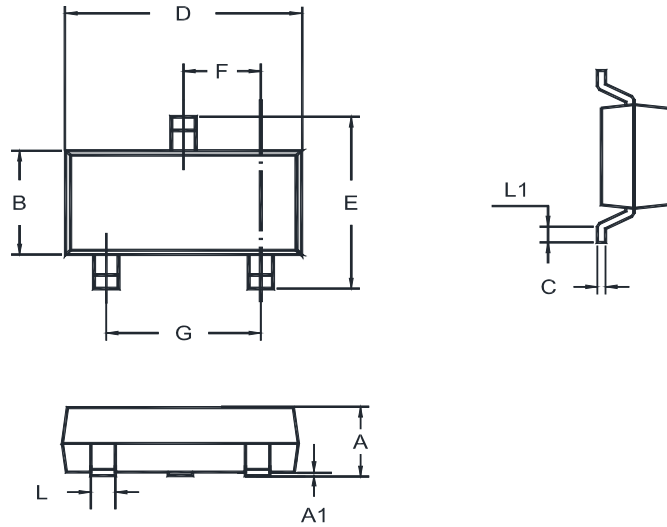
Fig.2-2 Gate charge waveform



MKA10N560L

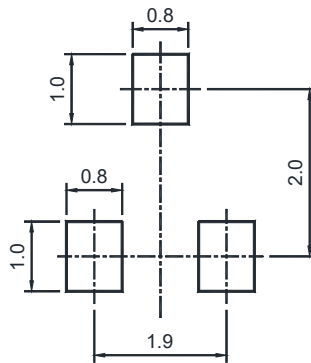
Package Outline (Dimensions in mm)

SOT-23



Unit	A	A1	B	C	D	E	F	G	L	L1
mm	1.20	0.100	1.40	0.19	3.04	2.6	1.02	2.04	0.51	0.2
	0.89	0.013	1.20	0.08	2.80	2.2	0.89	1.78	0.37	MIN

Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
SOT-23	8	4 ± 0.1	0.157 ± 0.004	178	7	3,000

Marking information

- " SY " = Part No.
 - " YM " = Date Code Marking
 - " Y " = Year
 - " M " = Month
- Font type: Arial

